OPERATOR'S & MAINTENANCE MANUAL

Model 278

12 MHz PROGRAMMABLE SYNTHESIZED FUNCTION GENERATOR

WAVETEK®

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12 MHz PROGRAMMABLE SYNTHESIZED FUNCTION GENERATOR

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Instrument Part Number: 1000-00-0185

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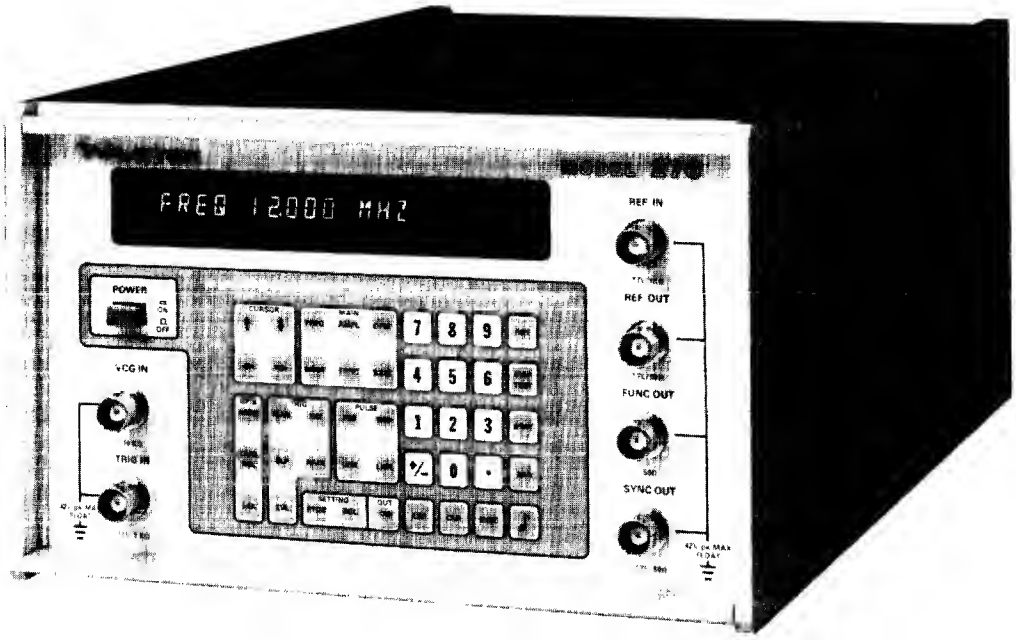
APPENDIX

SAFETY FIRST

Protect yourself. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with ⏚ or ⚠).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.



Model 278, 12 MHz Programmable Synthesized Function Generator

SECTION 1
GENERAL DESCRIPTION

1.1 MODEL 278

The Model 278, a 0.01 Hz to 12 MHz Programmable Synthesized Function Generator, can operate in continuous, triggered, gated, burst, synthesized, external reference, or external phase lock modes with output levels to 20 volts peak-to-peak.

The synthesized mode has 5 digits of frequency resolution with 0.0005% accuracy, or it can be locked to an external 10 MHz (zero-crossing or TTL) frequency reference for greater accuracy and stability. In addition, the separate synthesizer circuit acts as a highly accurate internal trigger source.

The generator can produce sine, triangle, square, square complement, and pulse waveforms as well as dc and external width..

Data entry is from the front panel or GPIB (IEEE-488, 1978). Numeric input is entered in free format: fixed, floating, or exponential notation. Parameters may be entered in any order. Internally, all entries are interactively checked for errors and displayed on the front panel, or they may be accessed through the GPIB.

Output level is specified from 10 mV to 10 Vp-p into a 50Ω termination and 20 mV to 10 Vp-p into an open circuit with 3 digits of resolution. Offset can be programmed to vary the waveform base line up to ±10V, or in the dc function, to vary the dc output.

All inputs and outputs are protected against short circuits and excessive voltages between ±15V. The function output is further protected against voltage inputs up to 140 Vac or ±200 Vdc. Activation of the protection circuits will cause a front panel error message and may cause a GPIB service request.

Up to 100 sets of complete front panel settings can be stored in memory. The memory has a non-rechargeable lithium battery back up for up to 6 months (typically 1 to 2 years). A "low battery" warning will be indicated on the display when the battery voltage drops to 80% of its normal voltage.

WARNING

This equipment uses a BR-1/2A, 3V lithium battery, that contains less than 0.3 grams of lithium. To prevent the release of a potentially harmful substance, DO NOT RECHARGE, SHORT CIRCUIT, DISASSEMBLE, OR APPLY HEAT TO THE BATTERY. In addition, observe correct polarity when replacing.

Instruments manufactured prior to serial number 7230039 may be limited to 40 sets of stored settings without battery back-up. But if an option (previously identified as Option 001) was installed, there will be a total of 100 sets of stored settings with non-rechargeable battery back-up as described in this manual.

1.2 ACCESSORIES

Rack mounts for a single instrument, rack mounts for two series 270 instruments side-by-side and instrument slides are available accessories. Refer to paragraph 1.3.16 for details.

1.3 SPECIFICATIONS

1.3.1 Waveforms (Functions)

Programmable sine ∿, triangle ∿, square ⊓, pulse ⊓, pulse complement ⊔, external width, and dc.

Sine Distortion (THD at 5 Vp-p)
<0.5%, 10 mHz — 99.9 kHz
No harmonics above
−40 dBc, 100 kHz — 999 kHz
−30 dBc, 1 MHz — 12 MHz

Time Symmetry
±1% ±8 ns.

Square Transition Time
<15 ns.

Square Overshoot
<4% at full amplitude

Triangle Linearity
99% to 100 kHz.

1.3.2 Operational Modes

Continuous
Output continuous at programmed frequency.

Triggered
Output quiescent until triggered by external signal, GPIB trigger, internal trigger, or manual trigger, then generates one cycle at programmed frequency. Trigger sources include 1 Hz to 24 MHz internal trigger generator in nonsynthesized modes.

Gated
As Triggered mode except output is continuous for the duration of the gate signal. The last cycle started is completed. Internal gate signal produces 50% duty cycle gate at trigger rates below 12 MHz. Not valid during pulse operation.

Burst
As Triggered mode for programmed number of cycles.
Count Range: 1 to 1,048,200.
Burst Rate: 12 MHz maximum

Synthesized
Same as Continuous except 5 digit frequency resolution and 0.0005% accuracy (5 ppm).

TTL Reference
Same as Synthesized except synthesizer externally referenced to a 10 MHz TTL source at REF IN BNC.

Zero Reference
Same as TTL Reference except external source is a zero-crossing 10 MHz signal.

TTL Lock
Main generator phase locked to external TTL signal at REF IN BNC. Capture and lock range >5% of programmed frequency.

Zero Lock
As TTL lock mode with external zero-crossing signal at REF IN BNC.

1.3.3 Frequency

Range
10 mHz to 12 MHz except 10 Hz minimum in synthesized modes.

Resolution
5 digits in synthesized modes. 3 digits in all other modes.

Accuracy
5 ppm ± 1 mHz in Synthesized mode. Accuracy of external signal ± 1 mHz in reference modes. ± 2% in all other modes.

Noise Floor
< −50 dBc.

Spurious
Typically < −45 dBc.

Repeatability (24 hr)
0.0003% in synthesized mode. ±1% in all other modes.

Jitter
≤0.1% ± 100 ps.

Control
Frequency may be controlled 3 ways: Value, VCG, or External Lock.
Value: Frequency value is keyboard or GPIB programmable with automatic range selection.
VCG (Voltage Controlled Generator): Ac or dc input controls frequency. 0.02 to ± 12V into 10kΩ for up to 1200:1 frequency change in each of 9 frequency ranges (ranges must be programmed).
Slew rate is limited to 1.0 V/μs.
External Lock: Frequency is determined by an externally applied signal at the REF IN BNC.

1.3.4 Amplitude

Range
0.01 to 10 Vp-p into 50Ω (0.02 to 20 Vp-p into ≥ 50 kΩ) from main output. Absolute peak amplitude plus offset may not exceed 5V into 50Ω (10V into ≥ 50 kΩ).

Resolution
3 digits or 10 mV when absolute peak amplitude plus offset >0.5V; 3 digits or 1 mV when absolute peak amplitude plus offset ≤0.5V.

Accuracy
± 2% of programmed value and: ± 5 mV for 0.01 to 1V (peak amplitude + offset <0.5V), ± 20 mV for 1.01 to 10V.

Repeatability (24 hr)
± 1% ± 10 mV.

Flatness
For output at 5 Vp-p: 0.1 dB to 100 kHz, 1.5 dB to 12 MHz.

1.3.5 Offset

Range
DC or offset programmable from −5V to +5V into 50Ω (−10V to +10V into ≥50 kΩ). Absolute peak amplitude plus offset may not exceed 5V into 50Ω (10V into ≥50 kΩ).

Resolution
3 digits or 10 mV when absolute peak amplitude plus

offset >0.5 V, 3 digits or 1 mV when absolute peak amplitude plus offset ≤0.5V.

Accuracy
± 40 mV in dc function.

Repeatability (24 hr)
± 1% <20 mV.

1.3.6 Internal Trigger

Range: 1 Hz to 24 MHz.
Resolution: 5 digits.
Accuracy: 0.0005%.

1.3.7 Pulse Period

Range: 90 ns to 1 sec.
Resolution: 3 digits.
Accuracy: 0.0005%.

1.3.8 Pulse Width

Range: 45 ns to 0.5 sec.
Resolution: 2 digits.
Accuracy: 3% + 5 ns.

1.3.9 Upper/Lower Level

Upper level must be greater than lower level.
Range: ± 5V.
Resolution: 20 mV.
Accuracy: See amplitude and offset specifications.

1.3.10 Outputs

Function Output
Source of primary waveforms. Programmable to be On (source impedance 50Ω), Off High Z (>500 kΩ), or Off Low Z (∿50Ω).
Source Impedance: 50Ω.
Protection: Output protected to 140 Vac or 200 Vdc without replacement of internal fuse.

Sync Output
Sync signal is at programmed frequency and TTL level.
Level: ≤0.4V to ≥2.4V into 50Ω, ≤0.8V to ≥4.8V into ≥50 kΩ.
Source Impedance: 50Ω.
Timing: Concurrent with function output in square; lags sine and triangle by 90°.
Over/Undershoot: <10% into 50Ω.
Protection: Output protected from short circuit to any voltage between ± 15 Vdc.

Reference Output
1.5 Vp-p into 50Ω, TTL level into open circuit, 10 MHz internal reference when in synthesized mode.
Internal Trigger frequency when internally in Triggered, Gated or Burst Modes.
Protection: Output protected from short circuit to any voltage between ± 15 Vdc.

1.3.11 Inputs

External Trigger
Trigger of input circuit is programmable for a + or − signal slope and required threshold level.
Level: −10 to +10V.
Resolution: 20 mV.
Accuracy: ± 500 mv (for signals with less than 10V/µs slew rate).
Input Impedance: 10 kΩ.
Maximum Trigger Rate: 12 MHz (24 MHz for External Width).
Minimum Trigger Width: 20 ns.
Minimum Amplitude: 500 mVp-p to 1 MHz, 1 Vp-p to 24 MHz.

Protection
Inputs protected to ± 50V.

VCG In
Voltage control of generator frequency. See Frequency.
Range: 0.01 to ±12V.
Impedance: 10 kΩ.

Reference Input
Used to externally reference or phase lock the main generator.
Programmable Input Selection: TTL or 1 Vp-p minimum zero-crossing.
Input: 10 MHz for external reference, 10 Hz to 12 MHz for phase lock.
Protection: Input protected to ± 50 Vdc.

1.3.12 GPIB Programming

IEEE 488-1978 compatible. Non-isolated. Double buffered.

Address
0-30, keyboard or internal switch selectable. Internal switch can lock out keyboard selection. Power-up address is internal setting.

Subsets
SH1, AH1, T6, TE0, L4, SR1, RL1, PP0, DC1, C0, E1.

Interface Timing

Frequency	28 ms
Amplitude	16 ms
Offset	19 ms
Mode	17 ms
Waveform	8 ms
Execute	24 ms
Other	30 ms max

1.3.13 Stored Settings

Nonvolatile memory for 100 stored settings.

1.3.14 General

Environmental

Temperature Range: 25°C ± 10°C for spec operation, operates 0°C to 50°C, −50°C to + 75°C for storage.

Warm-up Time: 20 minutes for specified operation.

Altitude: Up to 10,000 ft for operation. Up to 40,000 ft for storage.

Relative Humidity: 95% at 25°C and at sea level (non-condensing).

Dimensions

21.7 cm (8.54 in.) wide (half-rack), 13.3 cm (5.25 in.) high, 39.4 cm (15.5 in.) deep.

Weight

6.8 (15 lb) net. 7.2 kg (16 lb) shipping.

Power

90 to 105, 108 to 126, 198 to 231, or 216 to 252 volts rms; 48 to 66 Hz; 1 phase; <50 watts.

1.3.15 Options

002: Rear Panel Connectors

Front panel BNC's relocated to rear panel.

1.3.16 Accessories

Style 12: Single Rack Adapter Kit

Allows right or left mounting in a standard 19 inch rack. 5¼ inches high.

Style 13: Dual Rack Adapter Kit

Allows any 270 series instrument to be mounted side-by-side in a standard 19 inch rack. 5¼ inches high.

Rack Slides

SECTION 2
INSTALLATION AND INTERFACE

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

The generator can be used as a bench instrument or rack mounted. The 278 can be converted to rack mounts in the field by using the following kits.

Rack Mount Kit	Part Number	Reference Drawing
Single Instrument (left and right mounting)	1101-00-1043	0102-00-1043
Dual Instruments	1101-00-1041	0102-00-1041
Rack Slides	1101-00-1042	0102-00-1042

NOTE

The rack slides can only be used with dual rack mounted instruments.

Whether used on a bench or in a rack, ensure that there is no impedance to air flow at any surface of the instrument. Before rack mounting, it may be desirable to perform the initial checkout (paragraph 2.2.5) to verity operation of all functions.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 120 Vac line supply and with a ½ amp fuse.

Conversion to other input voltages requires a change in rear panel fuse holder voltage card position and fuse (figure 2-1) according to the following procedure.

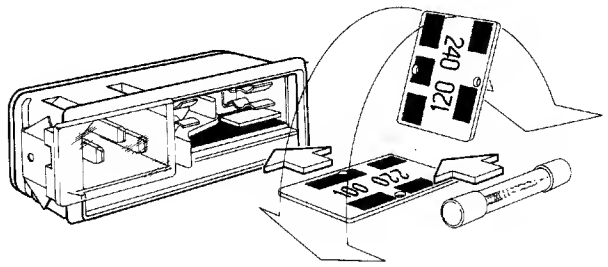


Figure 2-1. Voltage Selector and Fuse

1. Disconnect the power cord at the instrument, open fuse holder cover door and rotate fuse-pull to left to remove the fuse.

2. Remove the small printed circuit board and select operating voltage by orienting the printed circuit board to position the desired voltage to the top left side. Push the board firmly into its module slot.

Card Position	Input Vac	Fuse
100	90 to 105	3/4 amp
120	108 to 126	3/4 amp
220	198 to 231	3/8 amp
240	216 to 252	3/8 amp

3. Rotate the fuse-pull back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.

4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

2.2.2 Signal Connections

NOTE

Use RG58U or equivalent 50Ω coaxial cables equipped with BNC connectors to distribute signals.

Instrument BNC connectors are:

TRIG IN. Acceptable trigger level and slope are programmable; −10 to +10V, 10 kΩ impedance.

SYNC OUT. TTL level square wave; 50Ω impedance

FUNC OUT. Up to 10 Vp-p into 50Ω impedance; up to 20 Vp-p into >50 kΩ impedance.

VCG IN. 0.01 to 12V; 10 kΩ impedance.

REF IN. Acceptable reference input signal is dependent upon the selected mode (ref: paragraph 3.8.5). 10 kΩ impedance.

REF OUT. TTL level pulse. Output is dependent upon the selected mode (ref: paragraph 3.8.5). 50Ω impedance.

Signal ground may be floated up to ±42 volts with respect to chassis ground. Be aware that all signal grounds are common; thus, if one signal ground requires floating, all grounds must be floated together.

Table 2-1. GPIB Data In/Out

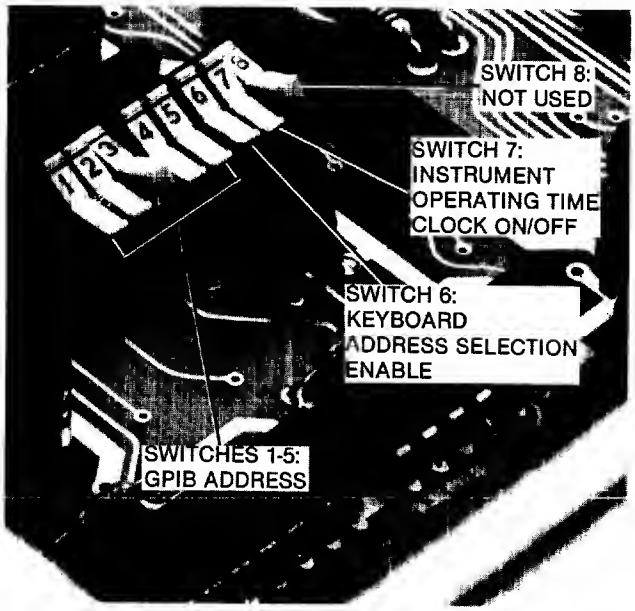
Pin	Signal	
1	DIO1	True When Low
2	DIO2	
3	DIO3	
4	DIO4	
5	EOI	
6	DAV	
7	NRFD	True When High
8	NDAC	
9	IFC	True When Low
10	SRQ	
11	ATN	
12	Chassis Ground	
13	DIO5	True When Low
14	DIO6	
15	DIO7	
16	DIO8	
17	REN	
18		Signal Gnd
19		
20		
21		
22		
23		
24		

2.2.3 GPIB Connections

The GPIB I/O rear panel pin connections and signal names are given in table 2-1. The panel connector is an Amphenol 57-10240 or equivalent and connects to a GPIB bus cable connector (available from Wavetek in 1 and 2 meter lengths).

2.2.4 GPIB Address

For instruments on the General Purpose Interface Bus (GPIB), ensure that the instrument GPIB address is correct. The GPIB address can be changed by the internal switch (for access, remove the bottom cover, see figure 2-2) or the front panel GPIB ADRS key (e.g., ADRS 4 EXEC). The switch sections are labeled from 1 through 5 and their OFF position noted (OFF = Binary "0" in table 2-2). To verify the address, press ADR on the front panel. The device number (decimal) will be displayed. Upon power-up, the address is always that of the internal switch.



NOTE: GPIB address selected is decimal 4: switch 1 Off, 2 Off, 3 On, 4 Off, 5 Off. (Table 2-2: 00100).

Figure 2-2. GPIB Address Selector Switch

Table 2-2. GPIB Address Codes

	ASCII		Switch Position	Hexa-decimal	
Device	Listen	Talk	1 2 3 4 5	Listen	Talk
0	(space)	@	0 0 0 0 0	20	40
1	!	A	1 0 0 0 0	21	41
2	"	B	0 1 0 0 0	22	42
3	#	C	1 1 0 0 0	23	43
4	$	D	0 0 1 0 0	24	44
5	%	E	1 0 1 0 0	25	45
6	&	F	0 1 1 0 0	26	46
7	'	G	1 1 1 0 0	27	47
8	(	H	0 0 0 1 0	28	48
9	)	I	1 0 0 1 0	29	49
10	*	J	0 1 0 1 0	2A	4A
11	+	K	1 1 0 1 0	2B	4B
12	,	L	0 0 1 1 0	2C	4C
13	—	M	1 0 1 1 0	2D	4D
14	•	N	0 1 1 1 0	2E	4E
15	/	O	1 1 1 1 0	2F	4F
16	0	P	0 0 0 0 1	30	50
17	1	Q	1 0 0 0 1	31	51
18	2	R	0 1 0 0 1	32	52
19	3	S	1 1 0 0 1	33	53
20	4	T	0 0 1 0 1	34	54
21	5	U	1 0 1 0 1	35	55
22	6	V	0 1 1 0 1	36	56
23	7	W	1 1 1 0 1	37	57
24	8	X	0 0 0 1 1	38	58
25	9	Y	1 0 0 1 1	39	59
26	:	Z	0 1 0 1 1	3A	5A
27	;	[	1 1 0 1 1	3B	5B
28	<	\	0 0 1 1 1	3C	5C
29	=	]	1 0 1 1 1	3D	5D
30	>	^	0 1 1 1 1	3E	5E

NOTE

Address 31 is not allowed.

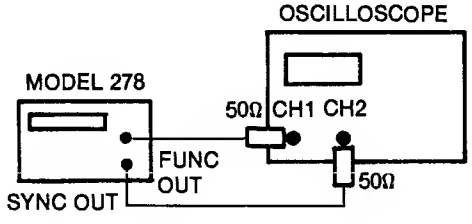


Figure 2-3. Setup

2.2.5 Initial Checkout and Operation Verification

Make the equipment setup as shown in figure 2-3 and perform the steps in table 2-3 to verify Model 278 operation. If further explanations are required, refer to figure 3-1 and table 3-1.

Table 2-3. Initial Checkout

Step	Test	Tester & Setup	Program	Desired Results
1	Wake-up State		Power: ON	Display: All segments, decimal points and commas light up for 1 sec (, typical of 20) then displays WAVETEK MODEL 278.
2	Wake-up Status		Press STAT key	Display (changes automatically): FREQ 1 KHz AMPLITUDE 5V OFFSET 0V MODE CONTINUOUS (0) FUNC SINE (0) BURST COUNT 2 PERIOD 1 ms WIDTH 45 ns UPPER LEVEL 2.5V LOWER LEVEL – 2.5V OUTPUT OFF (0) EXTERNAL TRIGGER (0) TRIG RATE 200 Hz TRIG SLOPE POS (0) TRIG LEVEL 1.5V
3	Status Search		STAT	Status display sequence stops.
4			↑	Status progresses forward.
5			↓	Status progresses backward.
6			STAT	Status display automatic sequence continues.
7	Display Test		DISP TEST	All segments, decimal points and commas light up. Back to last display when key released.
8	Beeper Test		Press FREQ key a few times	Beeper sounds everytime key is pressed.
9			Press ♪, then FREQ key a few times	Beeper is silent.
10			♪	Beeper enabled.
11	Command Recall		Press each of the 6 keys in the MAIN generator section 4 times then CMD RCL	Strings of characters shown on display. Characters are the ones shown on lower left of each key.
12			Press → then ←	Moves characters right then left 4 at a time.
13	GPIB Address And Status		ADRS 1 EXEC then 30 EXEC	Display: GPIB ADRS 1 then GPIB ADRS 30

Table 2-3. Initial Checkout (Continued)

Step	Test	Tester & Setup	Program	Desired Results
14	Quality Assurance Procedure	Connect Model 278 and oscilloscope as shown in figure 2-3. Scope setting: CH1 2 V/div, horizontal 0.2 ms/div; CH2 2 V/div; trigger on CH2.	Press: RCL 2000 EXEC	Display: (0) BEGIN QA PROC Scope: CH1 5 Vp-p 1 kHz sine wave CH2 2.5 Vp-p 1 kHz square wave
15	Frequency: Exercises Each Frequency Bit and the Sine Wave Function.		Press: CURSOR ↑ once.	Display: (1) FREQUENCY Scope: CH1 5 Vp-p sine wave continuously sweeping from 1 kHz to 10 kHz. CH2 2.5 Vp-p square wave synchronous with CH1.
16	Amplitude: Exercises Each Amplitude Bit and the Triangle Wave Function.		Press: CURSOR ↑ once.	Display: (2) AMPLITUDE Scope: CH1 1 kHz triangle wave, amplitude continuously increases from 1V to 10 Vp-p. CH2 2.5 Vp-p square wave synchronous with CH1.
17	Offset: Exercises Each DC Offset Bit and Square Function.		Press: CURSOR ↑ once.	Display: (3) OFFSET Scope: CH1 1 Vp-p square wave. DC offset continuously increases from −4V to +4V. CH2 2.5 Vp-p square wave synchronous with CH1.
18	Trigger Circuit	Trigger Scope on CH1.	Press CURSOR ↑ once.	Display: (4) TRIGGER Scope: CH1 single 5 kHz 5Vp-p sine wave. CH2 2.5 Vp-p 100 μs pulse, delayed 50 μs relative to positive edge CH1.
19	Gate Circuit		Press: CURSOR ↑ once.	Display: (5) GATE Scope: CH1 Burst of 6 cycles of 5 kHz sine waves CH2 2.5 Vp-p Pulse burst: six 100 μs pulses.
20	Burst Circuit		Press: CURSOR ↑ once.	Display: (6) BURST Scope: CH1 5 Vp-p sine wave continuously stepping from 9 to 2. CH2 2.5 Vp-p 100μs pulse continuously stepping from 9 to 2.
21	Quiescent State of Outputs		Press: CURSOR ↑ once.	Display: (7) END QA PROC Scope: CH1 Burst of 2 cycles of 5 Vp-p 5 kHz sine waves CH2 Burst of 2 cycles of 2.5 Vp-p 100 μs pulses.

SECTION 3
OPERATION

3.1 DATA ENTRY

Using the Model 278 is quite straight forward and is easily understood by trial and error. The microprocessor "converses" with you during operation, informing you what was programmed, what is possible to program, and when an error is made. Perform the procedures of table 2-3 to familiarize yourself with Model 278 operation. The keyboard is shown in figure 3-1 and cross referenced to table 3-1, which, in turn, references the applicable text. Readout that occurs when the keys are pressed are listed in Appendix C. When the operator starts keying in the parameter argument, no unit of measure is displayed until the parameter is terminated by a key other than a numeric entry key. Coded parameters, such as function, mode and output show their programmed argument in parentheses.

An audible tone indicates when a key is pressed. Pressing ♪ will prevent or restore the key tone. If there is no tone when keys are pressed, pressing ♪ restores the tone and vice versa.

Information exclusive to the GPIB is given in paragraph 3.16.

Additional reference information appears in the appendixes:

Appendix A - ASCII and IEEE (GPIB) Code Chart
Appendix B - Programming Command Summary
Appendix C - Displays
Appendix D - Output and Timing for Basic Modes and Functions.
Appendix E - Glossary of Mnemonics
Appendix F - Waveform Measurements

3.2 POWER

Power is turned on and off with a front panel pushbutton. When the power is turned on, the entire display lights up for a display element test. Then after about 1 second, "WAVETEK MODEL 278" is displayed.When the power comes on, the output is automatically disabled.

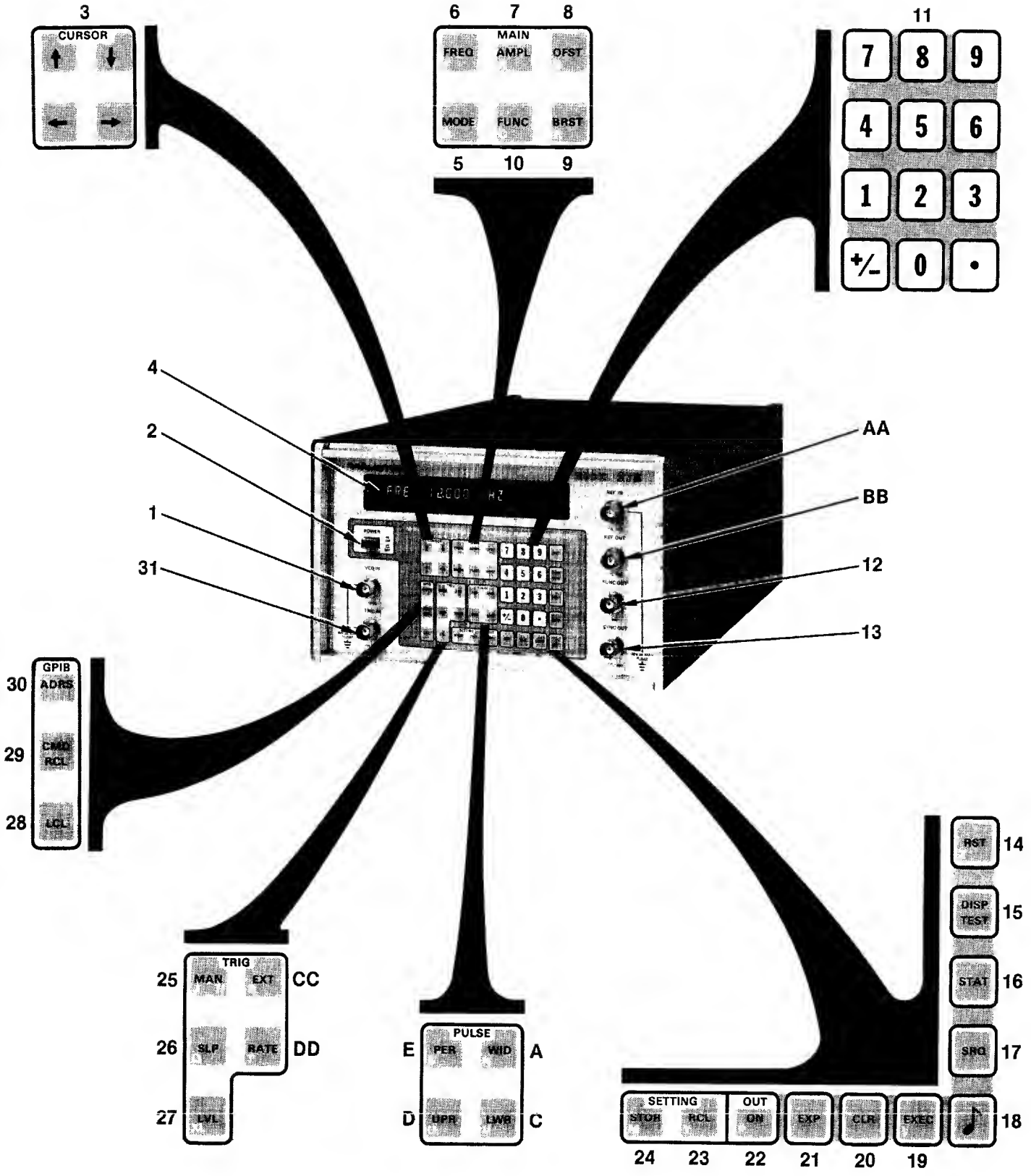
3.3 BASIC COMMAND STRUCTURE

The Model 278 is programmed by sending ASCII coded characters (ref: table 3-1 and Appendix A) to the microprocessor via one of the two possible input ports (keyboard or GPIB) shown in figure 3-2. If input characters are present on more than one input port, they are read first from the GPIB and then from the keyboard. Thus, if the GPIB port is continuously supplied with characters, then no characters will ever be read from the keyboard and the keyboard will appear inoperative to the user.

3.3.1 Characters

Characters used to program the 278 are divided into classes:

1. **Alphabetic Characters**—The characters A through Z (except E) select actions or commands. The X character used in front of another alphabetic character selects an alternate set of actions or commands. The X must directly precede the alphabetic character without intervening characters of any kind. For example, F selects frequency and XF selects percent frequency, but X F selects frequency not percent frequency because a space character, not X, was placed immediately before the F. Alphabetic characters are generated from the keyboard by pressing the labeled action and parameter keys. The characters generated by such keys are printed in a corner of the key.
2. **Numeric Characters**—The characters 0 through 9, E, −, and decimal point (.).
3. **Special Character**—Quote (') instructs the microprocessor to send to the display what is in quotes.
4. **Terminator Character**—Initially the ASCII line feed character (LF). This can be changed by programming (refer to paragraph 3.16.6).
5. **Nonprogramming Characters**—Any character not in one of the previously described classes.



NOTE: Features are keyed to Table 3-1

Figure 3-1. Controls and Connectors

Table 3-1. Function Cross Reference

Location in Figure 3-1	ASCII Character	Function	Action (A) or Parameter (P)	Paragraph
1	_____	VCG Input	_____	3.8.1.3
2	_____	Power	_____	3.2
3	_____	Cursor	A	3.6
4	_____	Display	_____	3.16.9
5	B	Mode	P	3.8.5
6	F	Frequency	P	3.8.1.1
7	A	Amplitude	P	3.8.2
8	D	Offset	P	3.8.3
9	R	Burst	P	3.8.6
10	C	Function	P	3.8.4
11	0 thru 9, •, ±	Number Characters	P	3.3.1
12	_____	Function Output	_____	3.11.1
13	_____	Sync Out	_____	3.10.4
14	Z	Reset	A	3.13
15	_____	Display Test	A	3.14
16	_____	Status	A	3.15
17	_____	Service Request	A/P	3.16.5.2
18	_____	♪(Tone On/Off)	A	3.1
19	I	Execute	A	3.5
20	_____	Clear	A	3.12
21	E	Exponent	P	3.3.3
22	P	Output On	P	3.11.2
23	Y	Recall Settings	P	3.10.2
24	M	Store Settings	P	3.10.1
25	J	Manual Trigger Pressed	A	3.7
25	H	Manual Trigger Released	A	3.7
26	Q	Trigger Slope	P	3.7
27	XL	Trigger Level	P	3.7
28	_____	Local Control Enable	A	3.16.8
29	_____	Command Recall	A	3.16.10
30	_____	GPIB Address	A	3.16.2.1
31	_____	Trigger Input	_____	3.7
A	N	Width	P	3.9.2
C	V	Lower Level	P	3.9.4
D	U	Upper Level	P	3.9.3
E	S	Period	P	3.9.1
AA	_____	Reference Input	_____	3.8.1.1
BB	_____	Reference Output	_____	3.11.5
CC	G	External Trigger	P	3.7
DD	T	Trigger Rate	P	3.7
_____	XU	Recall Next Lesser Numbered Program	A	3.10.2
_____	XW	Recall Next Greater Numbered Program	A	3.10.2
_____	XG	GET Mode	P	3.16.5.1
_____	XQ	SRQ Mode	P	3.16.5.1
_____	XT	Talk Message	P	3.16.4
_____	XV	Terminator Select	P	3.16.6
_____	XF	Percent Frequency	P	3.8.1.2

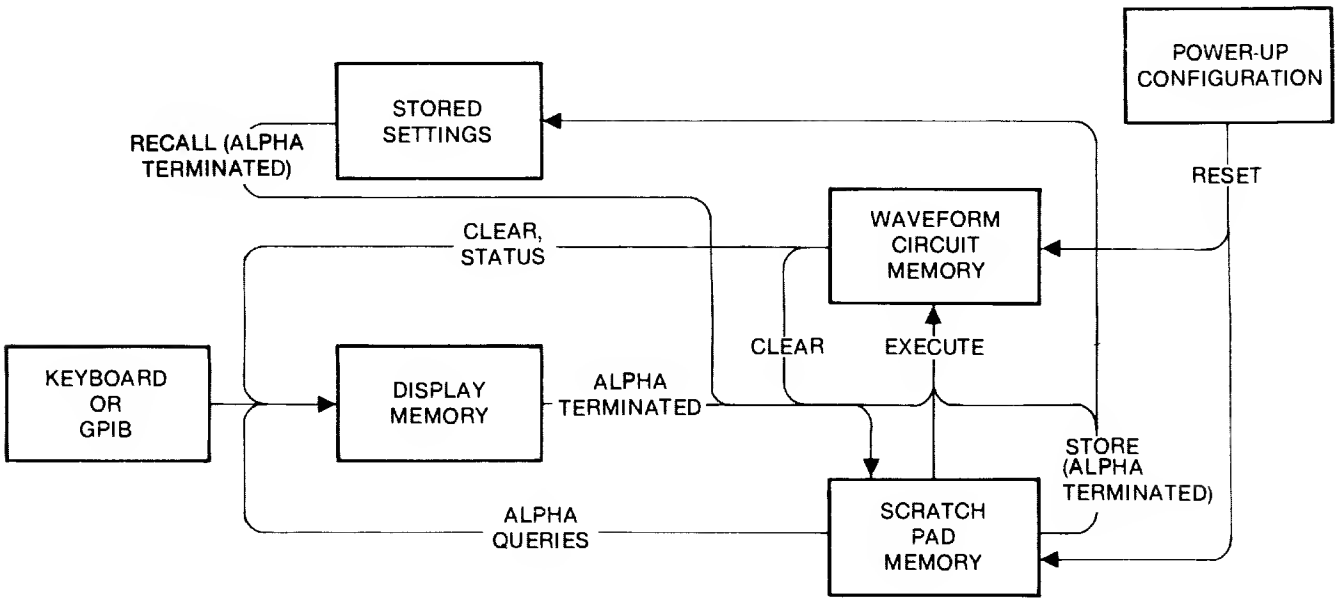


Figure 3-2. Memory Structure

They have no effect on programming and may be interspersed freely among programming characters, except after X (refer to item 1).

3.3.2 Action Vs Parameter

The alphabetic characters are used to select either actions or parameters (ref: table 3-1). An action is a sequence of events which happens when the letter that selects it is programmed or the key that selects it is pressed. There is no need for a numberical suffix. A programming parameter has one or two letters (and most have keys) plus a numeric value which controls some aspect of the instrument's operation.

To program an action, simply program the proper alphabetic character from either the front panel or GPIB port. The action will then take place, but only if the instrument is in the *enable* state at the moment when that character is read by the microprocessor (ref: REN, paragraph 3.16.1).

To examine the current value of a parameter, simply program the proper alphabetic character from either the front panel or GPIB port. The current value is then displayed on the front panel. Display occurs whether or not the instrument is enabled. If the character programmed does not correspond to a legal parameter in the instrument, nothing happens.

3.3.3 Programming Parameter Values

The numeric characters (0 through 9, E, −,) are used to program new parameter values. Data entry is free format; i.e., fixed point, floating point and exponential notation, or scientific notation.

Fixed Point — Decimal remains at far right.
Floating Point — You program the decimal point. It floats to the left in its designated position as you enter more numerals.
Exponential Notation — A value, then E followed by the exponent of a times ten multiplier. When the value (mantissa) is limited to one digit exponential notation is called scientific notation.

To change a parameter value, first program the alphabetic character which selects the desired parameter (F = frequency, etc.). Next, program the new value using numeric characters. Any sequence of characters which gives the new value is acceptable. For example, all of the sequences in table 3-2 cause the value 100 to be programmed.

The numbers to the left of the E are the mantissa; the digits to the right (only two are allowed) are the exponent. The result value is the mantissa times 10 to the

exponent power: for example 9.99 E2 = 9.99 × 10^2 = 999.

Table 3-2. Examples of Value Programming

ASCII	Keyboard	Standard Notation
100	100	100
0100	0100	100 (leading zeroes are ignored)
1E2	1 EXP 2	1 × 10^2
.01E4	.01 EXP 4	.01 × 10^4
.01E304	.01 EXP 304	.01 × 10^4 (last two exponent digits only are used)
1000E-1	1000 EXP ±1	1000 × 10^{-1}
1E-2-	1 EXP ±2 ±	1 = 10^2 (two minus signs cancel)
1E.2	1 EXP .2	1 × 10^2 (decimal points in exponent are ignored).

Only one decimal point and one E (keyboard EXP) are allowed per number; additional ones are ignored. The sign toggle character may appear any number of times. It causes the sign of the mantissa (if E has not been programmed) or the exponent (if E has been programmed) to be reversed (if negative, then positive, and vice versa) each time it appears. Any number of nonprogramming characters may be interspersed with the numeric characters, as they have no effect. If an undesired value is entered prior to execution (I or keyboard EXEC), the CLR key can be used to erase it.

Several parameters required codes for specific selections; for example, function codes 0 through 3 select sine wave, triangle wave, square wave and complement square wave. Refer to Appendix B for codes.

Since the number input format is so general, the microprocessor must be told when the last numeric character has been entered so it can evaluate the number. This is done by programming either an alphabetic, special or terminator character. When this is done, the new value is rounded off (ref: table 3-3) and tested to see if it is a legal value for the setting being changed (ref: paragraph 3.4). If it is legal, the new value is entered into the instrument's scratch pad memory; however, it is not yet sent to the waveform circuits. That is usually done by programming the I action (EXEC key on the front panel). Other methods of execution are GET and cursor, which are described later. An asterisk (*) on the display indicates that the new parameter value programmed has not been executed and resides in scratch pad memory only (ref: figure 3-2). All parameter values may be erased before execution by using the CLR key, the value stored in scratch pad is erased and the original value is displayed.

Table 3-3. Round Offs

Parameter	Round Off
Frequency	
Continuous	Up to 3 digits, 10 mHz minimum.
Synthesized, External Reference, and Phase Lock	Up to 5 digits, 1 mHz minimum
Amplitude and Offset	
Absolute peak amplitude plus Offset >0.5V	Up to 3 digits, 10 mV minimum
Absolute peak amplitude plus Offset ≤0.5V	Up to 3 digits, 1 mV minimum
Trigger level	Up to 3 digits, 20 mV minimum
Period	Up to 3 digits, 0.1 ns minimum
Internal Trigger Rate	Up to 5 digits, 0.1 mHz minimum
Width	Up to 2 digits, 10 ns minimum
Upper and Lower Level	Up to 3 digits, 20 mV minimum
All Other Parameters	To nearest integer

3.4 ERRORS

When an illegal value is programmed or interdependent parameter errors are detected, an error signal is indicated on the front panel or GPIB. Keyboard class 1, 2 and 3 errors are indicated on the front panel display and by a double "beep" of the key tone. For errors made via the GPIB (but not the keyboard), the service request line (SRQ) is asserted, providing a service request mode (XQ) has been selected (ref: paragraph 3.16.5). The controller can then serial poll its instruments to verify that the 278 sent the SRQ and can then inquire as to the nature of the 278 error. The method of reporting errors on the GPIB is given in paragraph 3.16.4.

3.4.1 Class 1 Errors

Class 1 errors are caused by programming values outside the legal limits of the parameter being programmed. For example, programming an amplitude of 500 volts will cause a parameter error when the next alpha character is programmed. At this time, the 278 disregards the new values and retains the previously programmed values in scratch pad memory (see figure 3-2).

3.4.2 Class 2 Errors

Class 2 errors are interparameter inconsistencies, such as the dc offset and peak amplitude greater than 5V into 50Ω. Tests are made every time an execute (I) is given, a setup is stored (M) or a cursor key is pressed. Resulting errors are displayed, and transfers of values are made to waveform circuits or storage regardless of the error indicated. Notice that upon receiving a Group Execute Trigger (ref: paragraph 3.16.7), the 278 programmng is executed without error checking.

3.4.3 Class 3 Error

Class 3 error occurs if an empty stored setting is retrieved. The error is displayed and the state of the 278 remains unchanged from the previously executed program.

3.5 EXECUTING THE PROGRAM

A program or setting can be executed, i.e., transferred to the waveform circuits by execute commands, GET (Group Execute Trigger) command, and the action keys: CURSOR ↑ and CURSOR ↓.

GPIB I and the front panel EXEC key are execute commands that cause parameter value and interparameter tests to be made and transfer the programmed values to the waveform generation circuits.

GET is a GPIB only command (no front panel key) that causes the 278 to execute and trigger, but without time consuming microprocessor error checks (ref: paragraph 3.16.7).

CURSOR ↑ and CURSOR ↓ are exclusively front panel functions which perform an execute with error checks after each digit increment or decrement.

GPIB **Z** and the front panel RESET are commands which reset the 278 to the original power up conditions (as described in table 2-3, step 2) and perform an automatic execute.

An asterisk (*) on the display indicates that the new parameter value programmed has not been executed and resides in scratch pad memory only (ref: figure 3-2).

3.6 CURSOR

The four cursor keys can modify a parameter value or code.

NOTE

The modified value is automatically executed.

The ← and → cursor keys move the cursor left and right; cursor position indicated by a flashing digit on the display. The ↑ and ↓ cursor keys increment and decrement, respectively, the flashing digit. Holding a cursor key down causes a continued change at a constant rate.

The ↑ and ↓ keys can also increment and decrement parameter codes, such as function and mode codes. Cursor positioning (← →) is not necessary for codes and codes do not flash to indicate cursor position.

When storing a program, press STORE key and then ↑. The program will be stored in the next memory location in numerical sequence. Keys ↑ and ↓ can also be used to recall stored settings in numerical sequence.

3.7 TRIGGER

The triggered and gated modes of the generator are initiated by a trigger signal. Triggers are: an external signal at the front panel TRIG IN BNC, an internal trigger source within the 278, a manual trigger using the front panel MAN TRIG key, or J (and H) commands via the GPIB.

G (or pressing EXT) followed by its code selects either external or internal triggering

G0 Selects external trigger.

G1 Selects internal trigger. When using internal trigger, use REF OUT BNC for a synchronization trigger output.

T (or pressing RATE) followed by its value selects the internal trigger rate. The rate can be programmed between 1 Hz and 24 MHz with up to 5 digits of resolution and 5 ppm accuracy.

J (or pressing MAN TRIG) is the start trigger for the main generator. In gated mode, the main generator is gated on.

H (or releasing MAN TRIG), in gated mode, terminates the output of the main generator. The last cycle started is always completed.

NOTE

Pressing manual trigger has no effect when internal trigger is selected.

Q followed by its code selects triggering either on the rising edge of the trigger signal or the falling edge.

Q0 Selects triggering on the rising edge (_/‾) of the trigger signal. When internal trigger is selected, the generator always triggers on the rising edge.

Q1 Selects triggering on the falling edge (⌝⌞) of the trigger signal.

XL followed by its value selects the signal trigger level. The value can be in the −10 to +10 Vdc range with 3 digit resolution. In internal trigger, selecting the trigger level does not affect generator triggering.

3.8 GENERATOR

The following sections describe the primary parameters related to generator operation. The block of keys envolved is labeled MAIN on the front panel.

3.8.1 Frequency

Direct frequency programming (nonsynthesized, synthesized, or phase locked), percentage frequency programming and voltage controlled frequency (VCG) are discussed in these sections.

3.8.1.1 Frequency (F)

Selecting **F** followed by a value programs, in hertz, the generator frequency.

Frequency resolution, accuracy and ranges depend on the selected operating mode, refer to table 3-4. For synthesizer modes with reference input (**5** and **6**) and phase lock modes (**7** and **8**), an external reference signal is required (ref: paragraph 3.8.5).

Table 3-4. Mode Affect on Frequency Accuracy and Resolution

Mode (Code)	Frequency Accuracy	Frequency Resolution
Continuous (0) Triggered (1) Gated (2) Burst (3)	±2%	Up to 3 digits
Synthesized (4)	±0.0005%	Up to 5 digits
Synthesized with TTL (5) or Zero Crossing (6) Reference Input	Accuracy determined by the reference source	Up to 5 digits
Phase Lock with TTL (7) or Zero Crossing (8) Input	Limited to accuracy of the external ref input	Frequency of external ref input

Each time a frequency is programmed the 278 microprocessor determines the best one of nine internal frequency ranges for operation. Each frequency range and its limits are shown in table 3-5. Firmware automatically changes frequency ranges as necessary. These are ranges associated with ASCII **F** programming, as opposed to ASCII **XF** (ref: paragraph 3.8.1.2) programming or VCG (ref: paragraph 3.8.1.3) operation.

3.8.1.2 Percent Frequency (XF)

XF, a GPIB exclusive parameter, followed by a value (0 to 100) programs frequency in percent of frequency range (0 to 100% in 0.1% increments).

Internal to the 278, there are nine decade ranges as shown in table 3-5. Maximum frequency is limited to 100% of a range; for example: the 10^6 range is limited to 10 MHz. The minimum frequency can be programmed to 0% with derated frequency accuracy. At 0% the actual output frequency may be 0 Hz.

In synthesized modes, percent frequency can only be used between 10% and 100% of the selected frequency range.

3.8.1.3 VCG Frequency

A signal, either dc or ac, applied to the VCG IN BNC can be used to externally control the frequency of the FUNC OUT signal. A positive voltage applied to the VCG IN connector will increase the generator frequency within a range, and a negative voltage will decrease the frequency within a range.

Frequency, using the VCG IN, can only be changed within a frequency range. Table 3-5 shows the nine frequency ranges, internal to the 278, and the limits for each range.

Figure 3-3 illustrates the VCG voltage required to change the programmed frequency to a desired output frequency. Frequency range must be selected before applying the VCG signal. For example, if 500 Hz is programmed, the 278 selects the 10^2 range (ref: table 3-5). As shown in the example of figure 3-3, the "Frequency Mantissa of Program" is 5 and a 5V "VCG IN" changes the "Frequency Mantissa of Output' to 10. Since operation is in the 10^2 range, output frequency is 1.2 kHz (max). Another example is a 1200:1 frequency sweep from 1 kHz to 1.2 MHz using 0.01 to 12.0 volt VCG signal. Table 3-5 shows that the frequency range is 10^5. To get in that range, program a value in the 10^5 "F" range. Next, program **F0**, from which, the 0.01 VCG voltage will cause the output to be 1 kHz, and a 0.01 to 12 volt VCG input will cause a 1 kHz to 1.2 MHz frequency sweep.

Table 3-5. Internally Selected Frequency Ranges

RANGE NAME	ACTUAL RANGES (Hz)* "F" RANGES**	"XF" RANGES	VCG RANGES
10^6	1.00M - 12.0M	0 - 10.0M	10.0k - 12.0M
10^5	100k - 999k	0 - 1.00M	1.00k - 1.20M
10^4	10.0k - 99.9k	0 - 100k	100 - 120k
10^3	1.00k - 9.99k	0 - 10.0k	10.0 - 12.0k
10^2	100 - 999	0 - 1.00k	1.00 - 1.20k
10^1	10.0 - 99.9	0 - 100	100m - 120
10^0	1.00 - 9.99	0 - 10.0	10.0m - 12.0
10^{-1}	100m - 999m	0 - 1.00	1.00m - 1.20
10^{-2}	10.0m - 99.9m	0 - 100m	100μ - 120m

* "F" ranges are applicable to keyboard and GPIB operation where parameter **F** is used.
"XF" ranges are applicable to GPIB operation where percentage frequency parameter **XF** is used.
VCG ranges are applicable when external voltage is used to control frequency.

** Firmware automatically selects "F" ranges regardless of the format used in programming frequency. In synthesized and phase lock modes, the 10^{-1} and 10^{-2} ranges are not applicable.

A VCG input should not be used in synthesized or phase locked modes.

3.8.2 Amplitude

An **A** followed by a value (up to 3 digits) programs the amplitude at the function output. Amplitude is programmed in volts peak-to-peak from 10 mV to 10 Vp-p specified into a 50Ω load. See table 3-2 for value programming, table 3-3 for round offs, and paragraph 3.11 for function output.

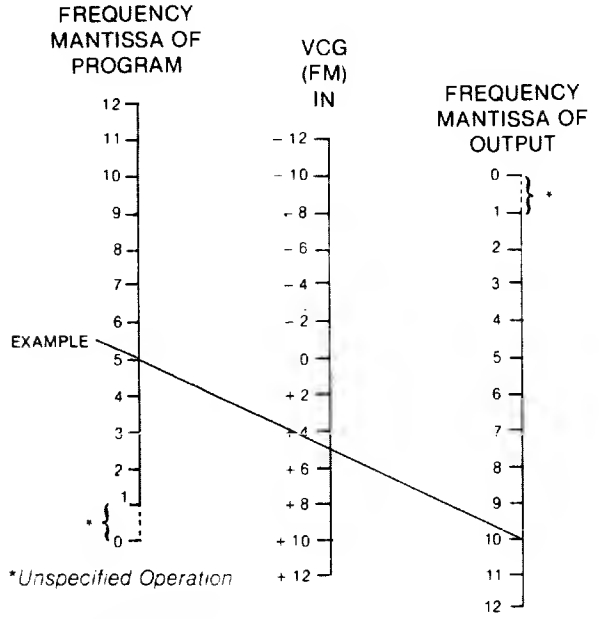


Figure 3-3. VCG (FM) Nomograph

Amplitude and offset resolution is dependent upon the sum of the peak amplitude and offset voltages. When the peak amplitude plus the offset voltage is greater than 0.5V, amplitude and offset resolution is limited to 10 mV. Yet, the amplitude and offset resolution is 1 mV when the peak amplitude plus offset is less than 0.5V.

3.8.3 Offset

D followed by a value (up to 3 digits) offsets the function output from 0 to ±5V specified into a 50Ω load. Offset is programmed in volts dc. See table 3-2 for round offs, and paragraph 3.11 for function output and load operation. Offset value may be modified by the cursor (ref: paragraph 3.6).

Amplitude and offset resolution is dependent upon the sum of the peak amplitude and offset voltages (ref: paragraph 3.8.2).

3.8.4 Function

C followed by a single digit parameter value selects function at the FUNC OUT BNC. Eight function codes are used.

C0 Selects sine wave.

C1 Selects triangle wave.

C2 Selects square wave in phase with SYNC OUT.

C3 Selects complement square wave 180° out of phase with SYNC OUT.

C4 Selects dc output voltage. The dc level is set by programming offset as described in paragraph 3.8.3.

C5 Selects external width. In external width, the output pulse period and width is fixed by the trigger signal (internal or external), while output level is adjustable by normal programming (ref: figure 3-4).

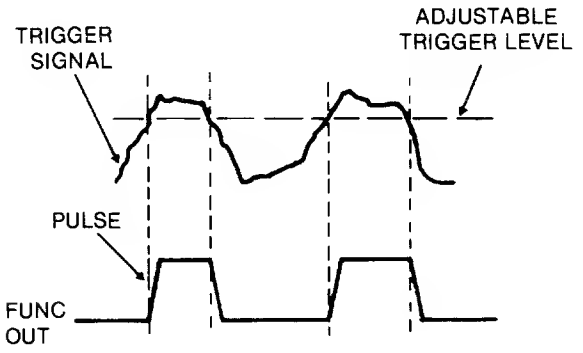


Figure 3-4. External Width

External width requires no mode selection but, in external trigger, requires trigger slope and level selection (ref:paragraph 3.7).

Pulse width is between the manual trigger push and release, ASCII **J** and **H** via the GPIB, or TRIG IN signal crossing and recrossing the trigger level value.

External width, when internal trigger is selected, requires selection of a triggered mode. Trigger rate programs the external width pulse period (ref: paragraph 3.7).

C6 Selects a single pulse in phase with SYNC OUT.

C7 Selects a single pulse 180° out of phase with SYNC OUT.

3.8.5 Modes

B followed by its code (0 through 8) selects the operating mode. The selected mode is indicated on the front panel readout when the MODE key is pressed. Three modes depend on a trigger, and four modes require an external reference signal. Refer to paragraph 3.7 for trigger slope and level selection.

B0 Selects continuous operation of the main generator.

B1 Selects triggered mode. The generator is triggered by external signal, internal trigger, manual trigger, or GPIB commands. When triggered, one cycle is generated.

B2 Selects gated mode. The onset of the trigger, regardless of its source (ref: mode **B1**), enables the generator for the duration of the trigger signal plus the time required for the completion of the last cycle started.

B3 Selects burst mode. Burst is the output of a preprogrammed number of cycles each time the generator is triggered (ref: paragraph 3.8.6).

B4 Selects the synthesizer mode that uses the instrument's internal reference. In synthesized mode, the instrument operates the same as continuous, but with increased frequency accuracy (0.0005%) and resolution (5 digits).

B5 Selects a synthesized mode that requires an external 10 MHz TTL reference signal at the REF IN BNC.

B6 Selects a synthesized mode the same as TTL reference (B5), except a 10 MHz zero-crossing signal is required at the REF IN BNC.

B7 Selects a phase lock mode that requires an external TTL signal at the REF IN BNC. The display reads LOOP LOCKED when the correct reference signal is present and LOOP NOT LOCKED when the signal is incorrect. The external reference frequency must be within 5% of the instrument's programmed frequency.

B8 Selects a phase lock mode the same as a TTL lock (B7), except a zero-crossing signal is required at the REF IN BNC.

3.8.6 BURST

R followed by a value (1 to 1,048,200) denotes the number of cycles in a burst. Duration of a burst is dependent upon the programmed frequency. Burst can be internally or externally triggered.

3.9 PULSE

The following sections describe pulse parameter control for pulse operation. The block of keys involved is labeled PULSE on the front panel. Pulse parameters are defined in Appendix D. Gated is not valid during pulse operation.

3.9.1 Period

S followed by a value programs, in seconds, the pulse period. Periods are programmable from 90 ns to 1 sec with up to 3 digits of resolution.

3.9.2 Width

N followed by a value, in seconds, denotes the pulse width. Programmed pulse widths are 45 ns to 500 ms with up to 2 digits of resolution.

Pulse width is measured from the 50% point of the leading edge to the 50% point of the trailing edge.

3.9.3 Upper Level

U followed by its value, in volts, programs the upper peak of all functions except dc. The upper level has a voltage range of −4.98 to +5V with up to 3 digits of resolution. The upper level must always be more positive than the lower level.

3.9.4 Lower Level

V followed by its value, in volts, programs the lower peak of all function except dc. The lower level has a voltage range of −5 to +4.98V with up to 3 digits of resolution. The lower level must always be more negative than the upper level.

3.10 STORED SETTINGS

Up to 100 different sets of front panel settings can be stored in and recalled from Random Access Memory (RAM). Nonvolatile memory is battery backed for 6 month (minimum) retention of settings.

3.10.1 Storing Program Sets

Program sets may be stored by keyboard or GPIB command. To store the program set that is in scratch pad memory (ref: figure 3-2), enter **M** followed by the storage location (1 through 100). The next alpha programmed is the terminator, which allows the storage to occur. If a program was previously stored in that location, it will be erased and replaced by the new set. When a program is stored, the settings are tested for errors in the same manner as with an execute command (ref: paragraph 3.5). The program is always stored, whether or not errors were detected. Programs can be stored without interrupting the output of the 278 if a terminator other than EXEC (I) is used: this is possible because it is the scratch pad memory that is stored rather than the actual settings of the waveform circuits (ref: figure 3-2). Notice that during 278 operation, scratch pad memory can be changed and stored without affecting 278 output.

3.10.2 Recalling Stored Programs

The information stored in a program may be recovered either from the front panel or by a command over the GPIB. To recall, program a **Y** followed by the number of desired program. When the next alpha entry is made, the settings stored in the selected program are transferred to display memory and the scratch pad memory (ref: figure 3-2). Then data is available to be sent to the waveform circuitry of the instrument, or, if desired, it may be examined and altered by use of the front panel keys.

The identifying numbers of programs in RAM range from 1 through 100. If the number of a program which does not exist or an illegal identifying number is programmed, an error will result.

A special location, RCL 0, contains the last executed settings. When power is turned off, RCL 0 contains the last executed settings prior to power off.

Pressing the cursor ↑ key or programming **XW** causes the program next in sequence after the last program accessed to be recalled. This provides an automatic way to recall a sequence of programs. However, the programs need not be numbered consecutively. If there is no program following the last program accessed, an error occurs.

Pressing the cursor ↓ key or programming **XU** is similar to the cursor ↑ or **XW** action previously described, except that programs are recalled in descending numeric order.

3.10.3 High Speed Recall of Stored Programs

The Group Execute Trigger (GET) allows a rapid GPIB recall of stored programs. In the GET mode of operation, the program is recalled and executed, and the waveform circuits are triggered, all within 2.5 ms of receiving the GET command. There are three possible modes of GET operation (ref: paragraph 3.16.7). There is no error checking in GET mode.

3.10.4 Deleting Programs

To delete a program, program the letter **M** followed by a *minus* sign and a number (except 0) of the program to be removed. When the number is terminated (by the next alpha character), the program is removed from storage; there is no other effect.

3.11 OUTPUTS

3.11.1 Function Output

At power-up and reset the FUNC OUT signal is turned off.

3.11.2 Output On/Off

P followed by a code switches the output on or off.

P0 Internally disconnects the signal from the FUNC OUT BNC (as described in paragraph 3.11.1) making the signal unavailable at the connector. In **P0**, the function output presents a high source impedance at the BNC.

P1 Internally connects the signal to FUNC OUT BNC.

P2 Internally disconnects the signal from FUNC OUT making the signal unavailable. The function output source impedance is approximately 50Ω.

3.11.3 Output Protection

The function output is protected from short circuits and external overvoltages over 200 Vdc or 140 Vac without damage to internal circuits.

Overvoltages are handled by using two methods: an overvoltage protection circuit and an output protection fuse.

The overvoltage protection circuit will detect external voltages (greater than ±15 Vdc but less than ±200 Vdc or 140 Vac) at the function output BNC and disconnect the output amplifier from the function output. The disconnection time is approximately 2 ms, but time can vary depending upon the level of the external voltage.

The output protection fuse will blow when an external voltage exceeds 200 Vdc or 140 Vac. When the fuse is blown, the display shows OUTPUT FUSE BLOWN, providing the function out is terminated with 50Ω, during one of the following cycles: after selecting Reset, at power up, after output on/off, or during the internal protection check. If the fuse is blown, remove the top cover, pull out the fuse (located at the rear of the main board), turn the fuse over and insert it. If the display continues to read OUTPUT FUSE BLOWN, replace with a new fuse block (Wavetek part number 1208-00-0977).

3.11.4 Sync Outputs

The SYNC OUT is a 0V to approximately 5V (TTL) signal from a 50Ω source. SYNC OUT is coincident with FUNC OUT. Timing relationships are shown in Appendix D.

3.11.5 Reference Output

The reference output is a 10 MHz TTL level pulse in the synthesized mode (B4). When internal trigger is selected in either the triggered (B1), gated (B2) or burst (B3) modes, the REF OUT will be a TTL level signal at the same frequency as the internal trigger ratio (ref: paragraph 3.7).

3.12 CLEAR ENTRY

The CLR key erases a parameter value which is being entered. The key removes the numeric digits entered after the last parameter letter entry but prior to execution. A clearable entry can be identified by either of two methods: an asterisk preceding the parameter or a cursor line (_) following the last number. The display is replaced by the previous value (scratch-pad value) of the parameter being programmed.

3.13 RESET

The RST key returns the 278 waveform parameters to their power-on condition. The readout becomes "RESET". Significant parameters values and conditions are given in table 2-3, step 2.

3.14 DISPLAY TEST

The DISP TEST key lights all 20 sets of character segments and semicolon as shown in table 2-3 step 1.

3.15 STATUS

Pressing STAT automatically displays the current waveform generator status one parameter and value at a time (ref: Appendix C). When STAT is pressed a second time the cycling immediately stops.The parameters can then be manually searched by using the CURSOR (↓ or ↑) keys (ref: table 2-3, steps 3 through 6).

3.16 GPIB

Almost all of the information in Section 3 is applicable to the General Purpose Interface Bus (GPIB) programming of the 278, but the information in this paragraph is *exclusive* to the GPIB.

The GPIB interface is an implementation of IEEE Standard 488-1978. It supports the following interface functions: SH1-Complete source handshape, AH1-Complete acceptor handshake, T6-Basic talker, TE0-No extended talker, L4-Basic listener, SR1-Complete service request (software select), RL1-Remote/local and local lockout, PP0-No parallel poll capability, DC1-Complete device clear/selective device clear, DT1-Complete device trigger capability, E2-Tri-state drivers. The talk capability allows a device to send data (such as error message readings) out over the bus. The listen capability allows a device to receive data (such as device programming information) from the bus.

3.16.1 Bus Lines Defined

The GPIB consists of 16 negative true signal lines:

DIO1 - DIO8	Data In/Out Lines
ATN	Attention

REN	Remote Enable
DAV	Data Available
NRFD	Not Ready For Data
NDAC	Not Data Accepted
EOI	End Or Identify
SRQ	Service Request
IFC	Interface Clear

1. **DIO1-DIO8**—These eight lines (Data IN/Out) are used to send commands from the controller and transfer data back and forth between instruments and the controller.
2. **ATN**—This line (Attention) is operated only by the controller. It specifies whether the information on lines DIO1 - DIO8 is data (ATN false) or a command (ATN true). Whenever ATN is set true, no activity is allowed on the bus except for controller-originated messages; additionally, every device connected to the bus is required to receive and process every command sent by the controller.
3. **REN**—This line (Remote Enable) controls whether devices on the GPIB are in local or remote modes. In local mode, devices respond to front panel commands and do not respond to GPIB originated commands. In remote mode, the situation is reversed: GPIB originated commands are obeyed, while front panel commands are ignored. The 278 enters the remote state when it receives its listen address (ref: paragraph 3.16.2.1) and REN is enabled. The 278 then stays in the remote mode until the REN line is put in the local state, a Go To Local (GTL) command is received or the LCL front panel key is pressed (ref: paragraph 3.16.2.4, item 4).
4. **DAV, NRFD, NDAC**—These are the "handshake" lines (Data Valid, Not Ready For Data and Not Data Accepted) which regulate the transmission of information over the lines DIO1-DIO8. For each command or data byte transferred, a complete handshake cycle occurs. This handshake is designed to hold up the bus until the slowest device has accepted the information.
5. **EOI**—When ATN is false, EOI (End Or Identify) indicates that the data on lines DIO1-DIO8 is the last byte of a data message. When the 278 receives a data byte with EOI true, the 278 automatically supplies a terminator character (ref: paragraph 3.16.6) following the data byte. When the 278 transmits the last byte of a message (which is always a terminator character), it also sets EOI true.
6. **SRQ**—This line (Service Request) is used by the 278 and other devices on the bus to signal the controller that they request attention. (Ref: paragraph 3.16.5). Since the SRQ line is common to all devices, additional tests must be made to determine which devices are signaling. The controller performs a Serial Poll to accomplish this.
7. **IFC**—This line (Interface Clear) is used by the controller to reset the interface logic in all devices connected to the bus to a known initial state.

3.16.2 Commands

Commands are sent over lines DIO1-DIO8 with ATN true. They are divided into five classes.

1. Listen Addresses
2. Talk Addresses
3. Secondary Addresses
4. Universal Commands

   DCL—Device Clear
   SPE—Serial Poll Enable
   SPD—Serial Poll Disable
   LLO—Local Lockout
5. Addressed Commands

   GTL—Go To Local
   SDC—Selective Device Clear
   GET—Group Execue Trigger

These commands and command groups are shown with their binary codes in Appendix A and further explanation follows.

3.16.2.1 Listen Addresses

Listen addresses are used to command a device to read any data bytes transmitted over lines DIO1-DIO8. There are 31 different available addresses (hexadecimal codes 20 through 3E, ASCII codes **SP** through >). A 32nd address, called unlisten (hexadecimal **3F**, ASCII ?), is used to command all devices to not read data bytes. The 278 listen address is selected by internal switches (figure 2-2) or by front panel keyboard; e.g., ADRS 1 EXEC for address number one. Either method of selection specifies the lower 5 bits of the address (ref: table 2-2). Pressing the front panel ADRS key displays the GPIB address as a decimal device number. At power-on the address is always that set by internal switches. Another internal switch (figure 2-2) can lock out address selection by front panel keyboard if desired. Each time ADRS is pressed, **XA** will appear in the CMD RCL string. The address can not be reprogrammed from the GPIB.

3.16.2.2 Talk Address

Talk addresses are used to command a device to transmit data over lines DIO1-DIO8 whenever ATN is false. There are 31 different available addresses (hexadecimal codes **40** through **5E**, ASCII codes @ through ^). A 32nd address, called untalk (hexadecimal **5F**, ASCII _) is used to command all devices to cease talking. The lower 5 bits of the 278 talk address are selected by the same switches used to select the listen address. Thus, if the 278 listen address is hexadecimal **21** (ASCII !), the talk address is hexadecimal **41** (ASCII **A**). Pressing the front ADRS key displays the GPIB address as a decimal device number.

3.16.2.3 Secondary Address

Secondary addresses are used following a talk or listen address to provide the ability to address more than the 31 devices provided for by simple talk or listen addresses. Secondary addresses are ignored by the 278.

3.16.2.4 Universal Commands

Universal commands are used to command a device to perform designated actions. Universal commands are recognized at all times. Universal commands performed by the 278 are:

1. **Device Clear (DCL)**—Resets the 278 to the initial power on settings. Refer to table 2-3, step 2 for power on conditions. DCL affects all devices on the bus. This information is also set into the waveform generating circuitry.
2. **Serial Poll Enable (SPE)**—Causes the instrument to enage in a serial poll by responding with the serial poll status byte when addressed as a talker. Data line DIO7 will be on, if service is being requested on the SRQ line. When the status byte is read, it is reset to an ASCII blank, and the SRQ line is released (of course, it may still be held down by other devices). The status byte is also available by reading the 278 talk message number 1. When this message is read, the status byte is reset and SRQ released as for the serial poll.
3. **Serial Poll Disable (SPD)**—Discontinues serial poll. Returns instruments to normal talk modes.
4. **Local Lockout (LLO)**—Causes the 278 to enter a state where the front panel LCL key is inoperative. In this state, the keyboard is disabled and the instrument will only accept parameter changes through the GPIB. To enable keyboard control, the GPIB controller must place the REN line in the local state.

3.16.2.5 Addressed Commands

Addressed commands are used to command a device to perform designated actions. Addressed commands are recognized only when the instrument is addressed as a *listener*. Addressed commands performed by the 278 are:

1. **Go To Local (GTL)**—Commands are 278 to go to the local mode (ref: to paragraph 3.16.1 for explanation of the REN line).
2. **Selective Device Clear (SDC)**—Resets the 278 to initial power on conditions. Refer to paragraph 3.13 for power on conditions. SDC affects only the selected unit.
3. **Group Execute Trigger (GET)**—Causes the actions specified by the GET mode (**XG**) code (ref: paragraph 3.16.7). If the 278 microprocessor is idle (i.e., not processing a previously sent programming string), a GET command will be completed) within 2.5 ms of receipt. Otherwise, it will not be done until current programming is processed.

3.16.3 Data Transfer

In addition to accepting programming characters, the 278 will transmit status information over the bus. To program the instrument, first send the listen address (with ATN on), followed by the programming data (in ASCII, with ATN off). The instrument microprocessor accepts the data as fast as possible, until either 64 characters are received or there is a pause during the transfer of data. At that time, the entire string of received characters is scanned by the microprocessor, which carries out the scan and accepts the next 64 character string. Whenever the microprocessor is finished scanning a string, the display will show the last parameter of the string. If the EOI line is asserted while sending a character to the 278, the currently programmed terminator character will be put into the input string following the character with the EOI.

3.16.4 Talk Mode

To read a message from the 278, send the talk address (with ATN on) over the bus. The instrument will then send the message currently selected by the Talk Mode (**XT**) setting. The last character of the 278's message will be the currently programmed terminator character with the EOI line asserted.

XT followed by a code (0 through 8) selects the kind of message the 278 will send when it is addressed as a talker on the GPIB.

XT0 Programming Error List (only errors from GPIB input). A typical error string is E 1F 2AD 3Y. Some error string characteristics are:

a. All error strings begin with E.

b. Most recent error is at the end of string.

c. Errors are separated by spaces.

d. Class 1 Error: A 1 followed by programming character that caused the error.

e. Class 2 Error: A 2 followed by the two conflicting program characters.

f. Class 3 Error: A 3 followed by M (Store) or Y (Recall).

g. Error strings can be up to 80 characters including E and blanks.

h. After transfer, the instrument clears the error string.

XT0 is the power-up talk mode.

XT1 Poll Byte Response: The byte sent if a serial poll was performed. The controller, by reading this byte, causes the instrument to clear the poll byte and reset the SRQ line if asserted. The poll byte sent is described in table 3-5.

XT2 The most recently selected parameter and its value. Example: FREQ 1E3. If no parameter is selected; e.g., power-on state or reset, then returns: NO PARAMETER SELECTED.

XT3 The entire instrument setup after last execute. Example: F1E3A5D0B0C0R2S1E-3N45E-9U2.5V-2.5G0T200P0Q0XL1.5 (the instrument setup immediately after a reset or on power up).

XT4 The instrument setup when execute is received; same format as **XT3**.

XT5 Instrument Identification: WAVETEK MODEL 278 V(X.Y). X.Y identifies the software version number.

XT6 The time since the instrument was powered on. Example Time: 1.3. Unit of measure is hours with 0.1 hour resolution (6 minutes).

XT7 The accumulated operating time. Example: TOTAL TIME: 306.2.

NOTE:

Toggling switch 7 (figure 2-2) clears the instrument-operating-time clock. With SW7 on, the clock runs during power on. With SW7 off, the clock clears to zero.

XT8 The number of stored settings installed. For the 278: STORED SETTINGS 100.

3.16.5 SRQ (Service Request)

3.16.5.1 SRQ Mode

XQ followed by a value (0 through 255) selects the conditions under whch the 278 asserts the SRQ line and rsv bit. The equivalent binary value is a "mask" for the serial poll response byte (ref: table 3-6). The binary mask selects certain conditions that will be recognized as conditions that assert the SRQ line and rsv bit. All other conditions are ignored (masked).

Table 3-6 shows the serial poll response byte. Each of the 8 bits represent a condition that, if selected by the SRQ mode, will assert the GPIB's SRQ line and the serial poll byte's rsv bit. Each bit maybe selected individually or in various combinations. The rsv bit (bit decimal position 64) and the undefined bit (bit decimal position 32) will have no affect if selected.

For example **XQ1** dictates that the SRQ line and the serial poll byte's rsv bit are asserted when there is a program error; such as, frequency beyond the 278's limits. The serial poll response byte will be 01000001.

In another example, **XQ131** dicates that the SRQ line and the rsv bit are asserted when a program error has occurred, the output protection is enabled, or the SRQ key is pressed. The serial poll response byte will be 11000011.

XQ1 is the SRQ power up mode.

3.16.5.2 SRQ Key

The SRQ key is located on the front panel of the 278. To use the SRQ key, the 278 must be in the local mode and the SRQ mode bit weight 128 must be selected (ref: table 3-6). Under these conditions, pressing the SRQ key asserts the SRQ line of the GPIB.

3.16.6 End of String or Terminator Specification

XV followed by its argument designates a new End Of String (EOS) or terminator character. The argument is the decimal value of the ASCII character that is to be the new terminator: an EOS character recognized by the 278. Any ASCII character except NUL is accepted.

The terminator character has two uses. During output, it is appended to the end of every response to a

Table 3-6. Serial Poll Response Byte

Bit Decimal Position	Bit Binary Position*	Bit Name	Bit Description
128 (MSB)	1000 0000	SRQ Key	A front panel key (ref: paragraph 3.15.5.2).
64	0100 0000	rsv	Request for service.
32	0010 0000	Undefined	Undefined bit.
16	0001 0000	Reference Not Locked	Indicates the generator is not locked to the external reference signal.
8	0000 1000	Low Battery	Indicates a low battery level for memory back-up battery (ref: paragraph 3.10).
4	0000 0100	Fuse Blown	Indicates output amplifier fuse is blown (ref: paragraph 3.11).
2	0000 0010	Output Protection	Indicates output protection is tripped (ref: paragraph 3.11)
1 (LSB)	0000 0001	Program Error	Indicates a program error; it can be either class 1, 2 or 3 error (ref: paragraph 3.4).

**Binary Code: 1 = Selected*
0 = Not Selected

talk request on the GPIB. During input, it signals, the end of a group of programming characters. Since it is always recognized, even in a quoted string, it can be used to insure that the instrument is in a known state, so that following programming characters will be interpeted correctly.

At power on time, the EOS character is the line feed control character, ASCII character LF (10_{10}). When the 278 issues a talk message, the EOS character is the last byte sent. In addition, the End Or Identify (EOI) line is pulsed low (END message) during the EOS character transmission. If the GPIB controller does not look for the END message (EOI line low), and it does not recognize the Line Feed (LF) as a string terminator, a new EOS character will be needed. For example, to change the EOS character from an LF to a Carriage Return (CR), program **XV**13.

3.16.7 GET Mode

XG followed by its code selects what actions occur when a Group Execute Trigger (GET) command is sent to the 278. The code may be **0, 1** or **– 1.**

0 Upon receipt of GET, the programmed waveform values are transferred to the waveform generator circuits, and then the microprocessor sends a trigger pulse if the mode is not continuous. This is the same sequence of events that would occur if an execute, then a trigger action (**IJ**) were programmed, except that no error checking is done. GET mode 0 is the power up condition.

1 Upon receipt of GET, the stored setting next in sequence after the last stored setting accessed is recalled, if it exists. Then the actions described for code **0** are performed. This is the same sequence of events that would occur if a next setting, an execute and a trigger action (**XWIJ**) were programmed, except that no error checking is done.

– 1 Upon receipt of GET, the stored setting previous in sequence before the last stored setting accessed is recalled if it exists. Then the actions described for code **0** are performed. This is the same sequence of events that would occur if a previous setting, an execute and a trigger action (**XUIJ**) were programmed, except that no error checking is done.

3.16.8 Local

The front panel LCL key switches the GPIB interface

to the local mode if it is not locked out (ref: paragraph 3.16.2.4, item 4).

3.16.9 Display

The single quote character (') is used to program a string of characters to be displayed on the front panel display. Program a single quote, the characters to be displayed, followed either by another single quote or by the terminator character. When the second quote or the terminator is programmed, the first 20 characters programmed after the first quote are displayed on the front panel. If fewer than 20 characters are programmed, then blanks are added to fill the display.

Examples (∧ indicates a blank character)

Three Programmed Inputs

1. '20∧CHARACTER∧LIMIT'
2. 'THIS∧STRING∧IS∧TOO∧LONG∧TO∧DISPLAY∧ENTIRELY'
3. ' '
   (no characters in string)

The Resulting Displays

1. 20∧CHARACTER∧LIMIT∧∧
2. THIS∧STRING∧IS∧TOO∧L
3. (blank display)

3.16.10 Command Recall

Pressing **CMD RCL** displays the last 40 parameters, values and actions (all in ASCII Code) sent to the 278 from the keyboard and the GPIB. The display shows only 20 characters at a time, and the CURSOR ← and → must be used to see the entire 40 character program string.

SECTION 4
CIRCUIT DESCRIPTION

4.1 GENERAL DESCRIPTION

The Wavetek 278 Synthesized Function Generator consists of four major sections (figure 4-1): the microprocessor control section located on the microprocessor/power supply board, the operator interface located on the display board, the function generator section located on the function generator board, and the synthesizer, main loop, burst counter and control logic circuits located on the auxiliary board. Each of these major blocks is described briefly in this general description and then in more detail in following paragraphs.

4.1.1 Microprocessor Control

The microprocessor (figure 4-2) is the clearinghouse for all control operations. Through its software program in Read-Only-Memory (ROM), the microprocessor accepts commands from the front panel keyboard or the IEEE-488 General Purpose interface Bus (GPIB), then sends operating parameters to the function generator circuits and auxiliary circuits, stores these parameters in Random Access Memory (RAM), and controls the front panel display.

The microprocessor section contains the analog interface circuitry which decodes and holds status information for the function generator board. A sample-and-hold circuit provides four analog voltages to control the function generator. Power supplies in this section power all the circuits of the instrument.

4.1.2 Operator Interface

The operator interface located on the display board (figure 4-2), includes the front panel keyboard, the fluorescent display, decoders and drivers. The micro-

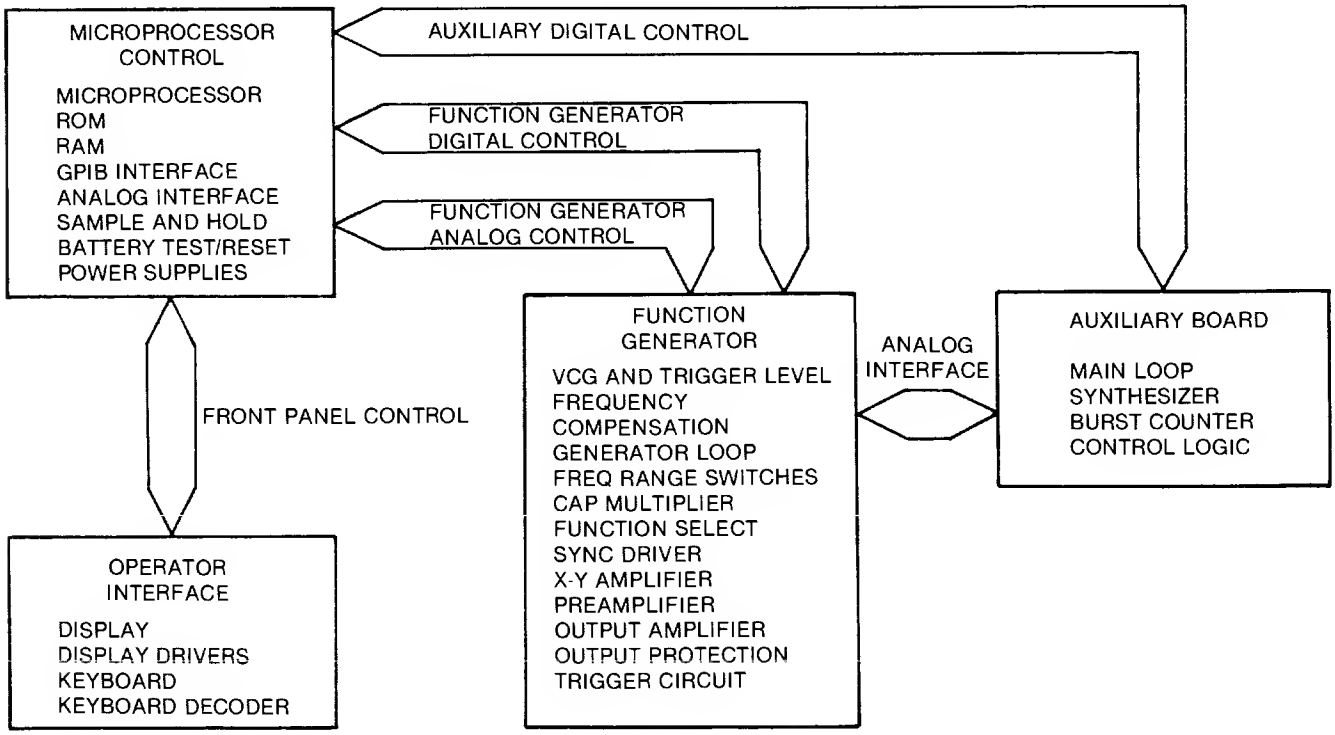


Figure 4-1. Major Blocks

processor recognizes entries from the keyboard and performs the appropriate instruction. Display drivers transfer display information from the microprocessor to the 20 character, vacuum-fluorescent alphanumeric display.

4.1.3 Function Generator

The basic generator loop, figure 4-2, creates a triangle waveform by alternately switching equal positive and negative currents into a capacitor. The switching points are determined by comparing the triangle peak voltages against two reference levels. A complement of the switching waveform controls the trigger timing in the mode logic, drives the square shaper, and is buffered to provide the instrument's synchronization output (SYNC OUT). Decade values of capacitors determine the basic ranges for frequencies from 100 hertz up. Below 100 hertz, a capacitance multiplier scales down the triangle current to provide the four lowest decades of frequency in the instrument.

Within any selected frequency range, a Voltage Controlled Generator (VCG) circuit varies the triangle current proportionally to the frequency control voltage (FRQ) from the microprocessor section. This circuit also controls high frequency compensation by proportionately decreasing the reference levels to compensate for time delays.

The function select circuit chooses a buffered triangle wave, a square wave derived from logic level signals, or a sine wave derived from the triangle wave. An X-Y multiplier circuit takes the current output from the function switch and, with its associated preamplifier, varies the waveform amplitude in proportion to the amplitude control voltage (AMP) from the microprocessor.

The output amplifier provides the final gain and output drive capabilities for the waveform, and sums offset from the amplifier into the signal as required. When the output signal peaks are programmed to be less than 1.0 volt, output voltage is attenuated by the decade output attenuator.

If excessive voltage is sensed on the output, the output protection circuit opens all the attennuator relays to protect the instrument. A voltage high enough to arc across the relays will blow a fast-acting fuse to further protect the instrument from major damage.

A trigger circuit allows the generator to be triggered or gated externally. An internal control voltage (TRL) controlled by the microprocessor determines the level at which an external signal (at TRIG IN) triggers or gates the generator. The external trigger signal can also be gated directly into the square shaper to provide an external width function.

4.1.4 Auxiliary Board

The auxiliary board contains the synthesizer, main loop, and burst counter circuits.

The synthesizer circuit generates an accurate frequency at either the programmed generator frequency or the programmed internal trigger rate. It can be referenced to either an internal crystal oscillator or an external reference applied to the REF IN connector. Trigger level for the external input is selectable for either TTL level or zero-crossing signals.

The main loop circuit phase-locks the function generator to either the output of the internal synthesizer or to an external frequency (applied at the REF IN connector) within 5% of the programmed generator frequency. Trigger level is selectable for either TTL or zero-crossing signals.

In the burst mode, the burst counter counts the square wave signal from the generator loop started by an external or internal trigger input. When a preset count is reached, the burst logic then turns off the generator through the normal gating logic.

The auxiliary board also contains control logic to latch data from the buffered data bus to control the other circuits on the board.

4.2 MICROPROCESSOR CONTROL CIRCUIT DESCRIPTION

The microprocessor control section and its associated circuits (figure 4-3) are located on the Microprocessor/Power Supply circuit board accessible beneath the bottom cover of the instrument. Descriptions in this section include the microprocessor/memory circuits, GPIB interface, battery test and reset circuitry, analog interface, sample and hold circuitry and instrument software.

The following descriptions refer to figure 4-3 and the microprocessor/power supply schematics in the back of this manual.

4.2.1 Microprocessor/Memory

The microprocessor/memory section includes the microprocessor itself, an address latch to demultiplex the lower order address bits, an address decoder to select appropriate memory locations or addressable registers, read-only-memory (ROM), random access memory (RAM), a data latch to hold data for transfer to analog and display registers, the beeper circuit, and the GPIB address switch and register.

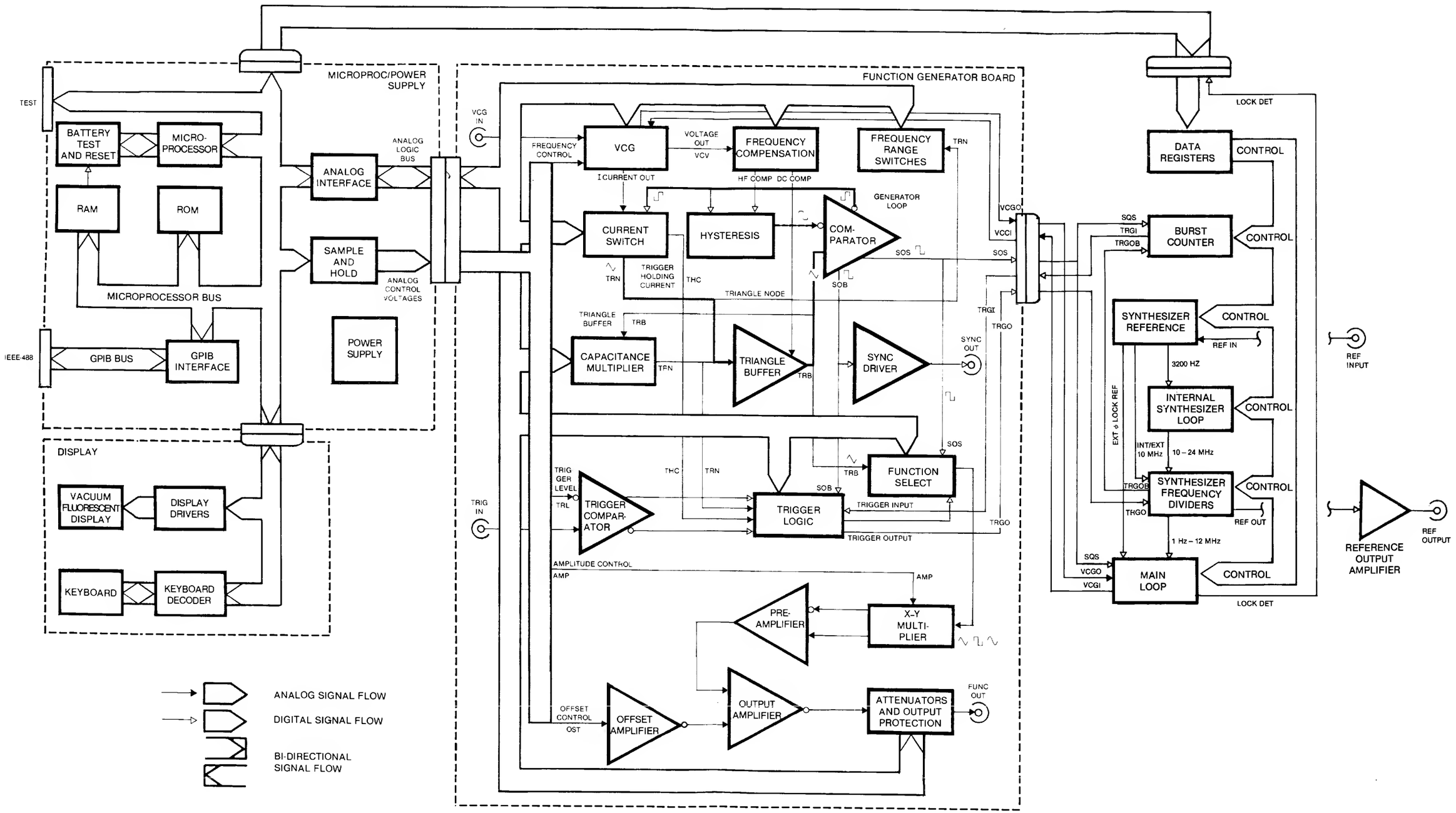


Figure 4-2. Functional Block Diagram

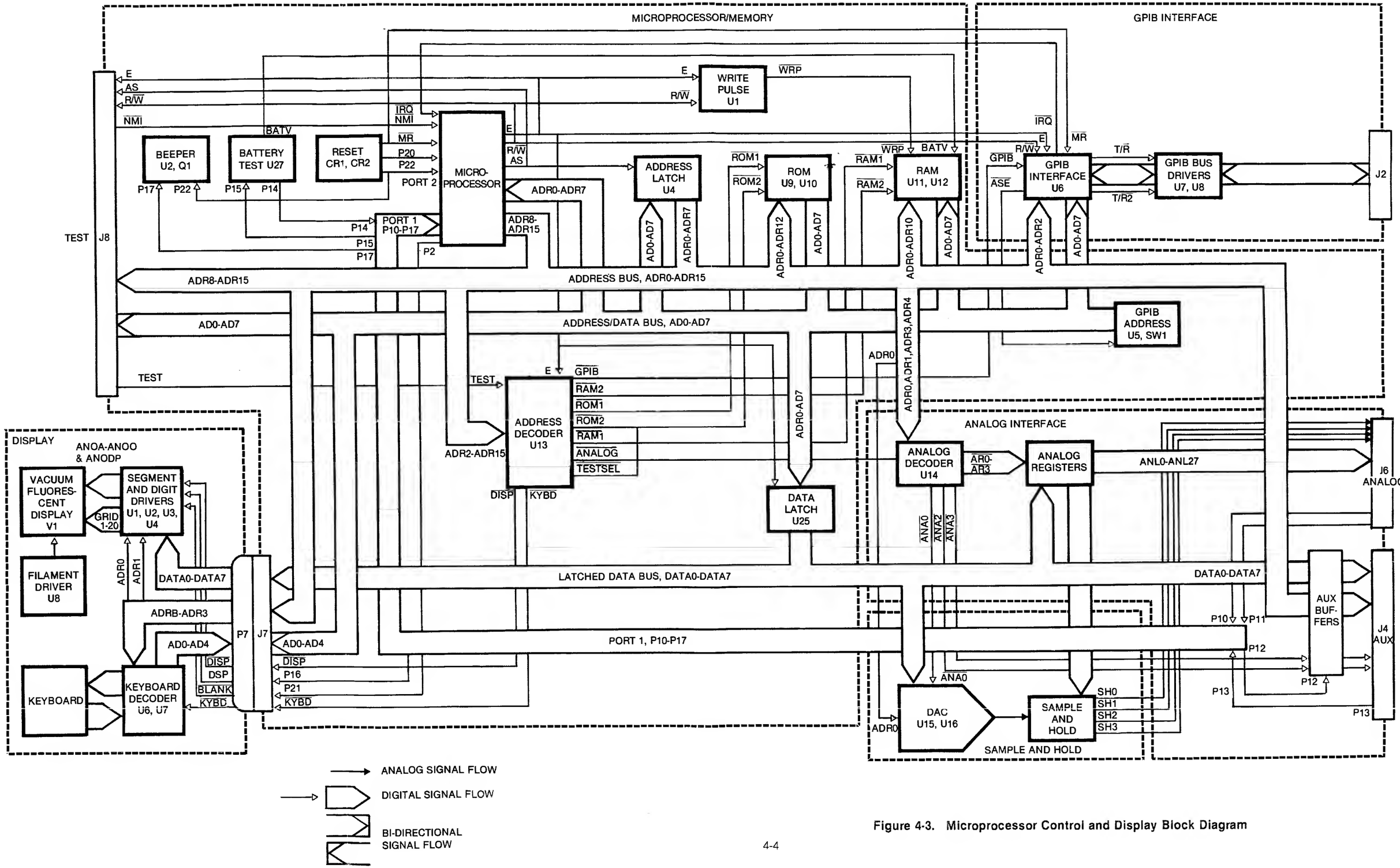


Figure 4-3. Microprocessor Control and Display Block Diagram

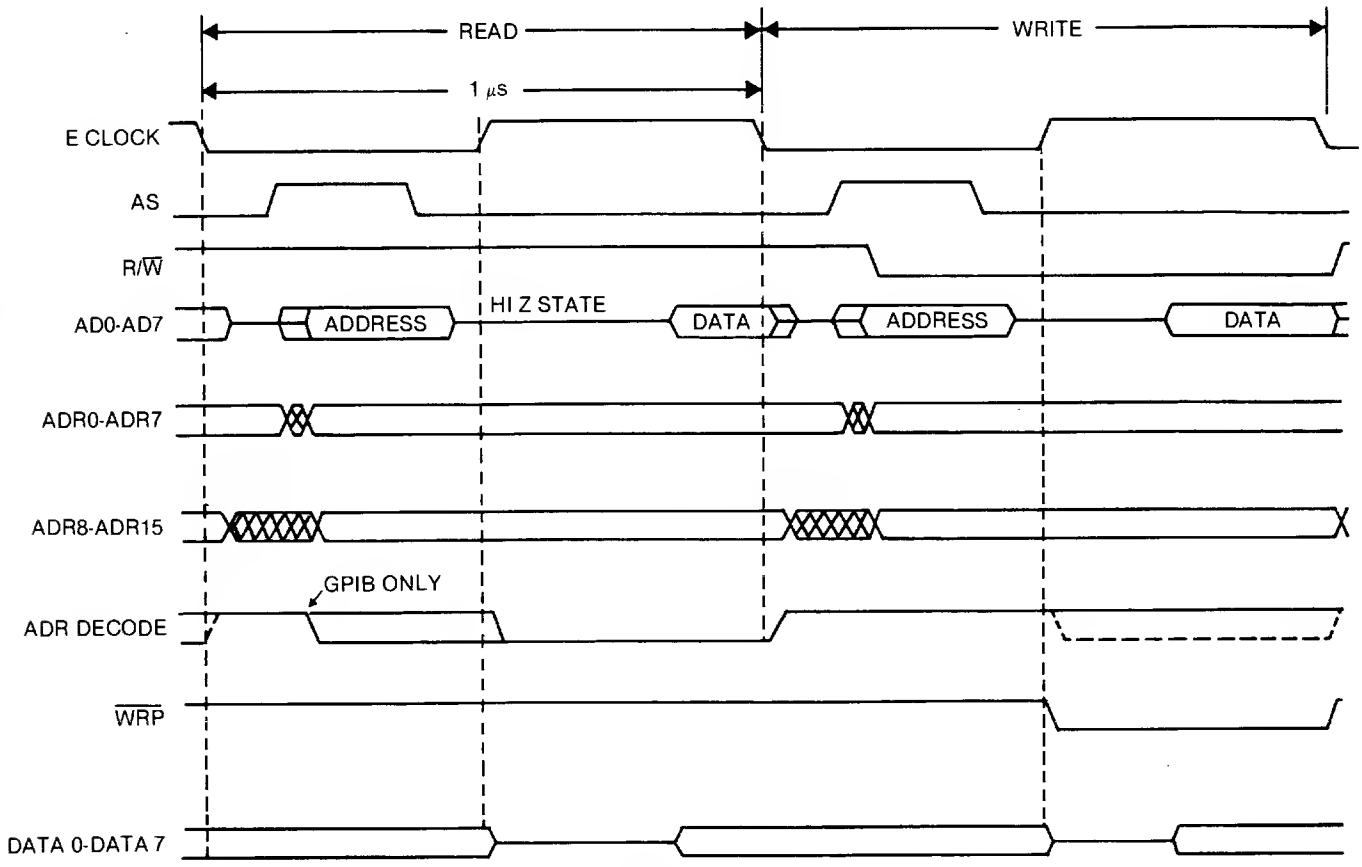


Figure 4-4. Microprocessor Timing Diagram

4.2.1.1 Microprocessor

The 6803 microprocessor, U3, is in its expanded-multiplexed mode (mode 2), as determined by mode control programming diodes, CR1 and CR2. This mode allows the microprocessor to address external memory by using port 3 (P30-P37) as the multiplexed low-order-address/data bus, port 4 (P40-47) as the high-order-address bus, with pins 39 and 38 as the address strobe (AS) and read/write line (R/W) respectively. Ports 1 (P10-P17) and 2 (P20-P24) are always I/O ports.

A clock-generating circuit within the microprocessor uses an external 4 MHz crystal, Y1, between the XTAL1 and XTAL2 pins to develop its internal phase clocks and the 1 MHz system enable clock (E). Figure 4-4 shows the approximate timing for major signals and busses in the microprocessor/memory system. Actual system timing varies somewhat from instrument to instrument, so signal spacing may be different within the 1μs period of the system clock.

The microprocessor responds to three interrupt inputs: master reset ($\overline{\text{RESET}}$), which initializes the microprocessor; the external interrupt request line ($\overline{\text{IRQ}}$), which the GPIB interface uses to signal the processor; and the non-maskable interrupt ($\overline{\text{NMI}}$), which is not used in the instrument, but is available on the test connector.

4.2.1.2 Address Latch

An octal latch, U4, demultiplexes the address/data bus from the microprocessor to hold the low-order addresses (ADR0-ADR7) during the part of the E clock cycle that data occurs on the multiplexed bus. Latching occurs on the negative transition of the AS signal (U3, Pin 39). See timing diagram, figure 4-4.

4.2.1.3 Data Latch

Octal latch, U25, demultiplexes data from the address/data bus much in the same way as the

address latch (U4), except that the falling edge of the E clock, rather than AS, latches the device.

4.2.1.4 Address Decoder

A field programmable gate array, U13, decodes the highest 14 of the 16 address lines to select one of eight possible addressable devices or circuits. These are the keyboard decoder (KYBD), display drivers (DISP), IEEE-488 interface (GPIB), RAM location 1 (RAM1), RAM location 2 (RAM2), ROM location 1 (ROM1), ROM location 2 (ROM2), and the analog interface registers (ANALOG). In addition, a ninth output decodes the reset and interrupt vector addresses into ROM2 for normal operation, but allows a test input to direct these vectors into external memory. A memory map, table 4-1, shows the position in memory for each of the above blocks.

4.2.1.5 ROM

Two read-only-memories, U9 (ROM1) and U10 (ROM2), contain the program for the microprocessor. Their respective locations in memory are adjacent as shown in the memory map, table 4-1. ROM1 and ROM2 from the address decoder enable the appropriate IC on the rising edge of E clock. A brief description of microprocessor operation will be covered in the software section.

4.2.1.6 RAM

The microprocessor uses two random access memories, U11 and U12, as a scratch pad memory and as memory for stored settings. The RAM1 or RAM2 line from the address decoder enables the selected RAM on the rising edge of the E clock. During a write cycle, the write pulse circuit AND's the read/write line from the processor (R/W) with the E clock to generate a write pulse (WRP) after all address lines have become stable. A lithium battery (BT1) maintains a sufficient voltage level to prevent the loss of information stored in both RAMs when external power is removed. Schottky diode CR5 conducts when the +5V supply falls below the battery's voltage (approximately 3V). Diode CR4 prevents the battery from discharging through the rest of the circuit.

4.2.1.7 Beeper

The microprocessor generates a 62.5 kHz signal continuously at port 22 (P22) after start-up producure is complete. To generate an audible beep, the processor sends a positive pulse from port 17 (P17) to the reset line of a 12-bit ripple counter, U2. The counter reset condition enables the 62.5 kHz signal from port 22 to the clock input of the counter. The fifth stage output of the counter drives a transistor switch which in turn drives the beeper at approximately 2 kHz. When the eleventh and twelfth stages of the counter both go positive, U1-3 inhibits the 62.5 kHz signal from the processor and stops the beeper. This gives a beep about 50 ms long.

Table 4-1. Memory Map

Addressable Devices	Address (Hexadecimal)
Internal Register	$0000 – $001F
Analog	$0020 – $003F
DISP, GPIB (See Note 1)	$0040 – $005F
KYBD & Not Used (See Note 2)	$0060 – $007F
Internal RAM	$0080 – $009F
Not Used	$0100 – $9FFF
ROM 1	$A000 – $BFFF
ROM 2	$C000 – $DFFF
RAM 1	$E000 – $E7FF
RAM 2	$E800 – $EFFF
Not Used	$F000 – $FFEF
Vector (ROM 2) (See Note 3)	$FFF0 – $FFFF

Notes

1. DISP $40 – $43, GPIB $58 – $5F
2. KYBD $60 – $6F, Not Used $70 – $7F
3. Alternate addresses for last 16 locations in ROM 2.

4.2.1.8 GPIB Address

An 8 section DIP switch (SW1), selects the GPIB address for the instrument. Since IEEE-488 specifications allow only 31 possible addresses for GPIB instruments (binary 0-30), only the first five switches S1-S5 (GA0-GA4), are used to select the actual address. S6 (FPADEN) enables or disables the front panel address entry capability. A momentary closure of S7 resets the elapsed operating time counter in the microprocessor. S8 is not used.

An inverting tri-state buffer, U5, gates the address switch information onto the multiplexed address/data bus when enabled by the address switch enable line (ASE) from the IEEE-488 interface device.

4.2.2 GPIB Interface

The GPIB Interface section of the microprocessor board interfaces with the instrument's microprocessor and handles all the handshake protocol and data transfer over the IEEE-488 General Purpose Interface Bus (GPIB).

Most of the IEEE-488 instrument bus protocol functions are handled by the General Purpose Interface Adapter (GPIA), a single IC, U6. Data and control portions of the bus require high current driving capability and specific line termination which the Bus Drivers, U7 and U8, provide. These two sections of the bus have different requirements depending on whether the instrument is acting as a talker or a listener: the data transceiver, U7A or U7B, always acts as a transmitter during talk modes and a receiver during listen modes, but the control transceiver requires that some lines transmit while others receive in both of these modes. These different requirements are met in the "A" transceivers by using different parts for each function (the 75160A for data and the 75161A for control) or in the "B" transceivers by using an extra control line (pin 11 on the 3447). The instrument is able to use either type of bus transceiver scheme.

The IEEE-488 Interface IC, U6, does all the handshaking requirements of the 1978 IEEE-488 standard. When the controller on the bus sends either the instrument's talk or listen address or a serial poll, U6 signals the instrument's microprocessor by asserting the interrupt request line, $\overline{IRQ}$ (a low on U6, pin 40). The processor can then interrogate any of the eight registers internal to U6. Data from the iEEE-488 bus (listen mode) is accessed by reading from the data register in U6; data output (talk mode) is written to the same register. The address strobe enable line ($\overline{ASE}$) from the interface IC, U6, controls the select line to U5 that enables the GPIB address switch, SW1. The microprocessor can read this switch by a read of the address register in U6, which causes U6 to set $\overline{ASE}$ low during the E-clock (data) portion of the microprocessor clock cycle. This address is not necessarily the address used by the interface IC (U6): that address is stored in U6 by writing into the internal address register.

During the microprocessor reset cycle (power up), $\overline{MR}$ to U6 pin 19 ($\overline{RESET}$) inhibits all the outputs to the bus drivers and the drivers themselves to prevent false information from being transmitted over the bus. In addition, to prevent a false service request message state (SRQ asserted), port 20 from the microprocessor scans the SRQ line at U6, pin 23 to keep a program monitor of the status of the SRQ flag out of U6. A false state could otherwise occur if a very fast controller addressed the instrument in quick succession before the instrument's microprocessor had time to reset SRQ.

For a complete definition of the GPIB lines, refer to paragraph 3.16 in the OPERATION section of the manual.

4.2.3 Battery Test and Reset

One-half of the dual operational amplifier, U27, acts as a voltage comparator to detect low voltage on the battery, BT1. When the microprocessor goes through its power up procedure and every six minutes thereafter, the processor strobes port 15 (P15) to a low state to simulate the battery's normal load when power is shut off, then checks the output of the comparator at port 14 (P14). If the battery voltage drops below +2.4V, the comparator goes high and the processor sets an internal flag. At power up, this flag causes an immediate display warning for low battery; after power up, a reset command, storing a stored setting or recalling a stored setting causes the warning display or an SRQ, depending on whether the command originates from the keyboard or the GPIB bus.

The second half of U27, acting as a comparator, serves as a microprocessor reset circuit. During power up, diode CR19 is reserved biased, allowing the positive input to U27 (pin 5) to rise to the voltage determined by R59 and R60: approximately +4.7V. With CR18 forward biased, the negative input to the comparator (U27, pin 6) rises more slowly, at the time constant determined by R57 and C72 (about a 100 ms). Since it takes about two time constants for the negative input to charge as high as the positive input, about 200 ms elapse before transistor Q2 is turned off and the $\overline{RESET}$ line to the microprocessor is allowed to rise. When power to the instrument is shut off and the +5V line begins to drop, diode CR18 is

reverse biased and the negative input to the comparator falls at the same rate as the +5V line. Diode CR19 is forward biased, so the voltage at the positive input falls more slowly. When the +5V line falls slightly below +4.75V, the comparator turns on Q2 and keeps the microprocessor reset as the power continues to fall.

4.2.4 Analog Interface

The analog interface consists of an analog decoder that decodes addresses in the analog section of memory, analog registers that hold digital information for the function generator board, and auxiliary buffers that route data to the auxiliary board.

4.2.4.1 Analog Decoder

When the microprocessor selects the analog section of memory ($\overline{\text{ANALOG}}$ goes low), a 2 to 4 line decoder (U14A) decodes the 32 bytes of memory from ADR3 and ADR4 into four, 8-byte blocks ($\overline{\text{ANA0}}$ – $\overline{\text{ANA3}}$). $\overline{\text{ANA0}}$ selects the digital-to-analog converter, U15. $\overline{\text{ANA1}}$ is decoded further from ADR0 and ADR1 by U14B to select the analog registers ($\overline{\text{AR0}}$ – $\overline{\text{AR3}}$). $\overline{\text{ANA2}}$ and $\overline{\text{ANA3}}$ select registers on the auxiliary board.

4.2.4.2 Analog Registers

The analog registers hold the analog control logic for the function generator board, ANL0 – ANL27, and the four sample-and-hold select lines. Latched data (DATA0 – DATA7) is strobed into registers U21 through U24 by the falling edge of the analog register control lines, $\overline{\text{AR0}}$ through $\overline{\text{AR3}}$, respectively. ANL0 through ANL27 appear at the analog connector, J6.

4.2.4.3 Auxiliary Buffers

The tri-state auxiliary buffers, U28 and U29, prevent the latched data lines from injecting noise through the auxiliary connector (J4) to the auxiliary board by inhibiting the buffers except when the auxiliary board registers are being addressed. One-half of U28 (input pins 2,4,6,8) is continuously enabled, but the signals at its inputs do not change until the microprocessor selects the auxiliary registers. At this time, the buffered port 12 (P12) enables the buffered data (BDATA0 – BDATA7) and buffered address lines (BADR0 – BADR2).

4.2.5 Sample and Hold

The sample-and-hold section consists of the DAC (digital-to-analog converter) U15, the −10.24V reference for the DAC, and four sample-and-hold circuits that demultiplex the DAC output to provide four separate analog control voltages for the function generator board.

4.2.5.1 DAC

The 10-bit digital-to-analog converter, U15, contains its own internal registers for latching data and interfaces directly to the latched data bus (DATA0 – DATA7). When the microprocessor transfers data into the DAC with ADR0 high (approximately every millisecond), the negative transition of $\overline{\text{ANA0}}$ latches the most significant 8 bits from the data lines into the DAC's internal register. A second transition of $\overline{\text{ANA0}}$ with ADR0 low latches the two least significant bits. The current output of the DAC (U15 pin 12) is converted to a voltage output by operational amplifier U16A at pin 1 using a feedback internal to the DAC at U15 pin 14.

4.2.5.2 −10.24V Reference

Since the DAC circuit provides an inverted programmable portion of the reference voltage, the reference must be negative to get a positive output. This adjustable negative voltage is generated by operational amplifier U16B in an inverting configuration with a gain of less than −1 and using the highly regulated +15V power supply as its input. R16 adjusts the voltage for precisely −10.24V corresponding to a 10 mV step for each binary step of the DAC.

4.2.5.3 Sample and Hold

The microprocessor sequences the DAC through four discrete voltages at about 1 ms each (4 ms for a complete cycle). The four sample-and-hold circuits latch each of these analog voltages in turn to provide the four separate analog control voltages to the function generator board, SH0 through SH3, appearing at J6. In the following paragraph, component designations refer to the first sample and hold section that generates SH0 (corresponding to frequency control, FRQ, on the function generator board). The other sample and hold circuits act similarly.

Within a few microseconds after the appropriate voltage appears at the output of the DAC circuit, the sample-and-hold control line from U24 pin 12 turns on the analog switch U17A and the DAC output charges the holding capacitor C28. Since the analog switch, U17A, transmits a small charge from its logic input (pin 1) to the analog output (pin 3), an inverter, U18F, generates an opposing signal and the capacitor, C27,

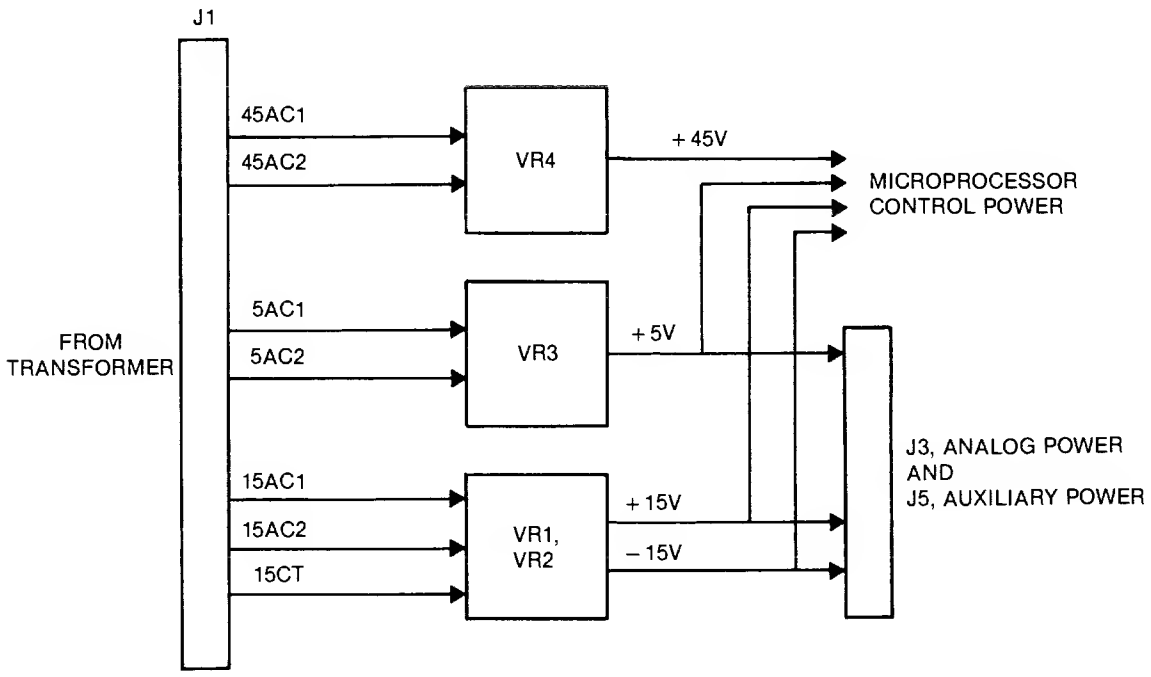


Figure 4-5. Power Supply

injects the opposite charge to cancel the effect. Because these charges do not exactly coincide in time, the result is a high-frequency bipolar spike that must be eliminated. A two-stage filter consisting of R18, C29, R19 and C30 accomplishes this. The holding capacitor C28 continues to charge until the next sequence is due. The control signal from U24 pin 12 turns analog switch U17A off before loading the following circuit's DAC information at U17D. The analog switch's high output impedance in the "off" state and the high input impedance of the buffer at U19B maintain the voltage on the output of the circuit with negligible discharge until the next cycle selects this sample-and-hold circuit again.

4.2.6 POWER SUPPLY

Four power supply voltages, +15V, −15V, +5V and +45V (figure 4-5) are generated on the microprocessor/power supply circuit board. The pass elements for each of the supplies are three-terminal regulators (VR1, VR2, VR3 and VR4) which normally operate with a 1.25V difference between their output and reference terminals. The +5V and +45V supplies use very little additional circuitry. In these simpler supplies, the reference voltages are provided by a resistor divider.

4.2.6.1 +5V Supply

In the +5V supply (Microprocessor/Power Supply Schematic, sheet 3), ac from the transformer, T1 (located on the rear panel), is rectified by CR13 and filtered by C56 and C57 to provide unregulated dc for the regulator, VR3. Resistive divider R49 and R50 sets the voltage at the reference input, pin 3, to provide an output of +5V ±5% at E2, while C58 and C59 provide additional filtering at the output of the regulator. R53 loads the supply to guarantee operation of the regulator if the +5V test jumper is removed. CR14 prevents C59 from discharging back through the regulator when power to the instrument is turned off.

4.2.6.2 +45V Supply

The +45V supply operates much the same as the +5V supply, except that the unregulated dc at VR4 pin 1 and the regulated output voltage (at pin 2) are much higher. The divider, R52 and R51, sets the output slightly below +45V so the 5% tolerance of the regulator cannot give an output greater than +45V.

4.2.6.3 ±15V Supplies

The + and − 15V supplies that power the analog sections of the instrument require greater accuracy

and stability than the basic regulator provides, so some additional circuitry is necessary. In the +15V supply, the operational amplifier, one-half of U26, compares a portion of the output voltage with a stable zener reference diode, CR10. The op-amp's inverted output drives the reference input of the regulator to compensate for any error in the output. Since the op-amp output cannot operate within 1.25V of its positive supply voltage, a divider, consisting of R35 and R36, allows the output to operate near ground potential. R33, which is in series with the output of the regulator, causes current regulation to take place at a lower value than the internal limiting that the regulator provides. As the current through R33 reaches its limiting value, the voltage drop across R33 reaches 1.25V, the normal voltage difference between the regulator output and reference pins. Any further current through R33 now creates a greater than 1.25V drop that the regulator senses at VR1 pin 3 as an overvoltage and responds by decreasing its output voltage until the current falls back to the limiting value. Diode CR9, in series with the op-amp output (U26 pin 1) prevents the op-amp from sourcing any extra current through R35 that would change the output current limit. A small current through R34 keeps the op-amp in its operating range up to the current limit. C69 and C70 speed up the external regulation to match the internal regulator. R39 allows the output to be adjusted to precisely +15V.

The −15V supply operates similarly to the +15V supply, but the polarities are reversed and the op-amp tracks the +15V supply rather than using another zener as a reference. R47 adjusts the −15V supply.

4.2.7 MICROPROCESSOR SOFTWARE

Although a detailed description of software is beyond the scope of this manual, some discussion of the microprocessor operation is helpful in understanding how the instrument functions.

Figure 4-6 shows the three main program loops for microprocessor operation: a fast background loop, a slow background loop, and the parser-procedure loop. The background loops only check registers for interrupt flags set by external or timer interrupts. The parser selects and calls procedures when the program enters it, and returns control to the fast background loop when a procedure is finished.

4.2.7.1 Fast Background

The fast background loop inspects the three internal registers (GPIB, keyboard and timer) for interrupt flags (non-zero states) and then returns to its beginning. If no interrupt flags are set, the entire loop takes only about 50 to 60 μs. If a flag is set, the loop time increases by the length of the interrupt procedure. If either of the first two register flags (GPIB or keyboard) are set, the background program calls the parser. When the parser completes an operation, it returns the program to the beginning of the fast background loop. If the timer register flag is set, the program enters the slow background loop.

4.2.7.2 Slow Background

The timer flag in the fast background loop looks for an overflow in the 2^{16} bit (which occurs about every 66 ms) of the timer counter (part of the microprocessor IC). The slow background loop then examines a series of other registers: GPIB address change, output protection flag, elapsed time (with its associated battery test timer), a status display timer, and an auxiliary board status flag.

Address Change. The GPIB address change actually compares two sets of two registers: it compares the stored keyboard-entry address, (if enabled) with the register in the GPIB interface and if they are different, enters the new value in the interface; it also compares the previously stored value of the internal address switch with the current setting of the switch, and if they are different, enters the new switch setting in the switch storage location, the GPIB interface, and the front panel register. In addition, if the keyboard entry is disabled, it inhibits the first comparison. The elapsed time counter is reset at this time if the reset section of the switch, SW1 (ETR) changes.

Output Protection Flag. The output protection flag initiates a short routine, when set, that displays the front panel output protection error message, sets SRQ in the GPIB interface, initiates an extended warning beep by repeating 32 beep activations spaced by a timer, and opens up all the output relays on the function generator board.

Elapsed Time Flag. The elapsed time flag is set at 6 minute intervals by the timer. It updates the elapsed time counter (adds 0.1 hr) and initiates the battery test timer. The battery test routine loads the battery for about 120 ms and then checks the battery test circuit for low battery voltage. If the battery is low, the routine sets a flag that causes a store, recall, or reset command to display a low battery warning, give a double beep, and set SRQ.

Status Display Timer. The status display timer works only when the instrument is set to display status. At intervals of about 1.17s, the timer flag is set and the

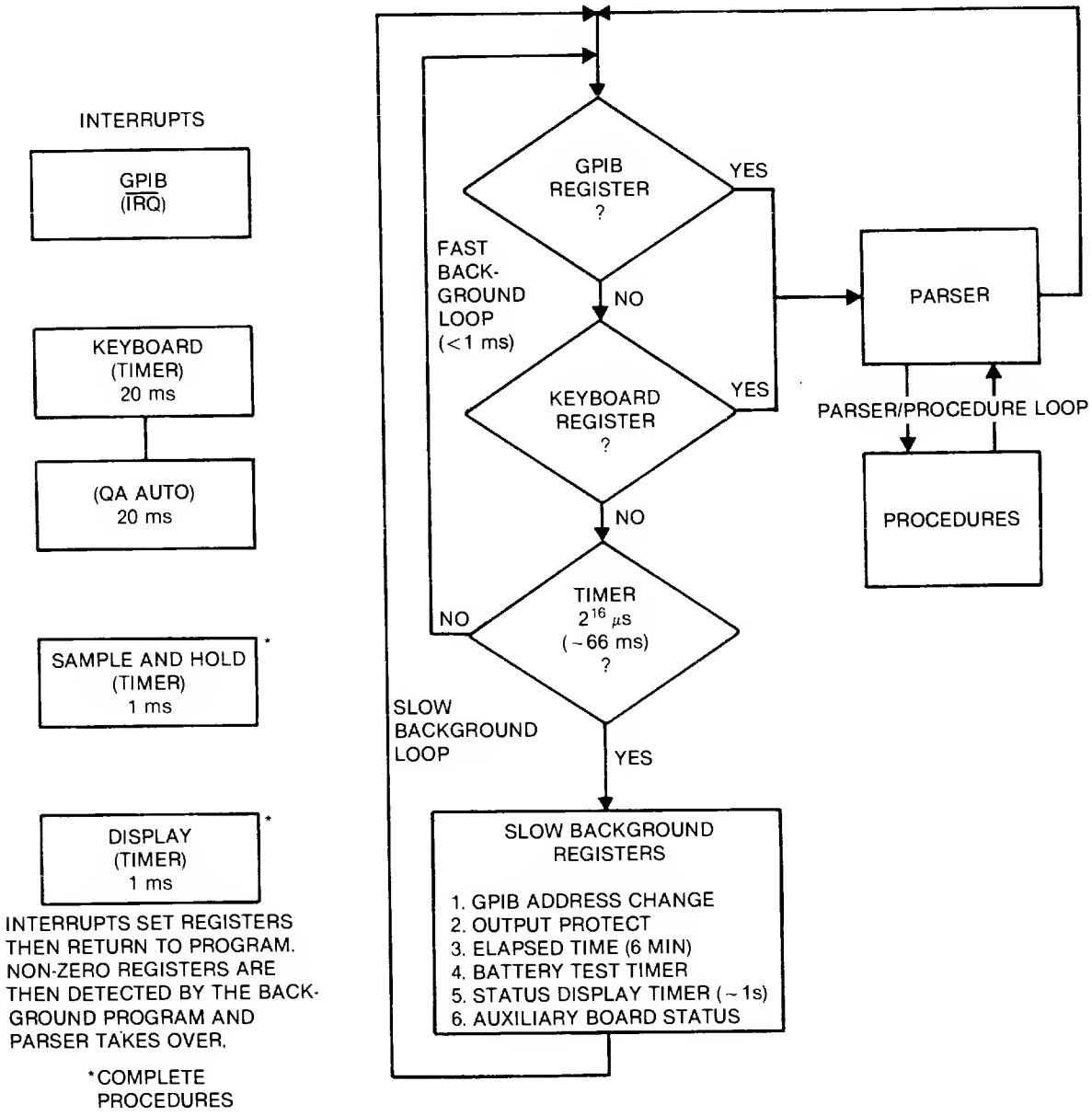


Figure 4-6. Program Loops

next background pass causes the equivalent of a cursor command to the instrument, advancing the status display.

Auxiliary Board Status. The auxiliary board status flag is set by a low on the LOCK DET line in the synthesized and phase-lock modes (modes 4-8) to cause a front panel warning that the **main** loop is unlocked. The front panel display also indicates when the **main** loop is again locked. However, the lock detect circuit will **not** indicate loss of lock in the **internal synthesizer** loop, such as might be caused by removal of the 10 MHz external reference in the external reference modes (modes 5 and 6). In most cases, the main loop will remain locked to the unlocked synthesizer.

4.2.7.3 Parser/Procedure

The parser handles all programming chores except short housekeeping routines. When the parser is called, it examines a series of registers and decides which routines are required, then calls the required procedure which, when complete, returns control to the parser. When the parser has scanned all the con-

dition registers, it returns control to the fast background. Even if their functions appear simple, the parser and the procedures with their interpretive functions make up the bulk of the program.

4.2.7.4 Interrupts

There are only two ways the processor program can be interrupted: through $\overline{IRQ}$ (generated by the GPIB interface) or through an internal timer (used for all other interrupt requirements).

GPIB Interrupts. GPIB interrupts are initiated by the GPIB responding to GPIB bus commands. When the interrupt occurs, a byte is read from the GPIB interface and stored in a register. The program then returns to its pre-interrupt position. It is the fast background program that actually inspects the register and passes control to the parser, which in turn decides what routines are called to process the information.

Timer Interrupts. Certain subroutines are run during initial power-up and periodically during the time the instrument is on. These subroutines are initiated when the number in the clock register (within the microprocessor) matches the preset number in any of the interrupt registers (within the microprocessor). Upon completion of the subroutine, the preset number corresponding to the elapsed time required between successive interrupts for the function is again added to that interrupt register. The clock timer continues to increment its own register, and when the number in this register again matches the interrupt register, the subroutine is initiated. These interrupt registers work independently of each other and may set another register (as in the keyboard interrupt) or they may initiate an entire subroutine.

4.3 OPERATOR INTERFACE CIRCUIT DESCRIPTION

The operator interface section is located on the display circuit board, which is mounted behind the front panel. Included are the display circuits (consisting of the segment drivers, digit drivers, the filament driver, and the display), and the keyboard circuits, (consisting of the keyboard decoder and the keyboard.

Refer to the display schematic in the back of this manual for circuits described in the following paragraphs.

4.3.1 Display

The display circuit consists of vacuum fluorescent display, V1, filament driver, U8, segment drivers, U1 and U2, and digit drivers, U3 and U4. The display is strobed on, one digit at a time, by the microprocessor.

The microprocessor controls the display multiplexing. A 1 ms timer interrupt initiates a display scan routine that advances one digit at a time on the display and enters the appropriate decoded drive information. After the twentieth digit (20 ms), the microprocessor resets an internal counter, and the digit scan repeats.

Figure 4-7 shows the digit timing sequence for the display. The interrupt timer in the processor sets $\overline{BLANK}$ (Port 21) low. Inverted by U5E, this signal disables all display drivers (which blanks the display) and advances the shift register in the digit drivers, U3 and U4. After about 200μs, $\overline{BLANK}$ returns to its high state and the appropriate digit is enabled (GRID1-GRID20). When the processor's scan counter reaches 20, it sets the digit scan position line.

During the time $\overline{BLANK}$ is low, the processor recalls the digit information already decoded for the 16 segment display and stores this data in latches within

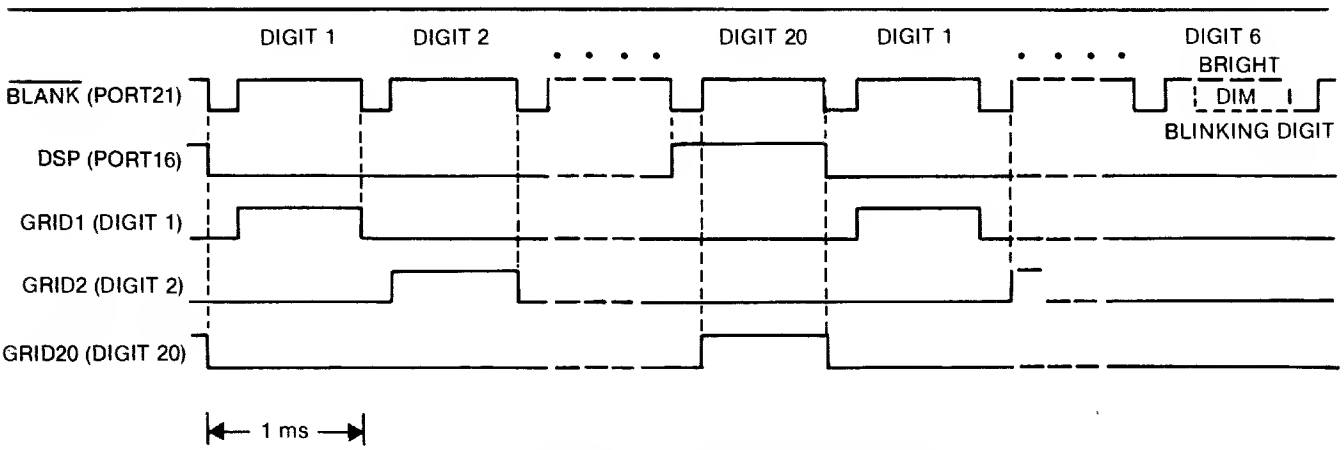


Figure 4-7. Display Digit Timing

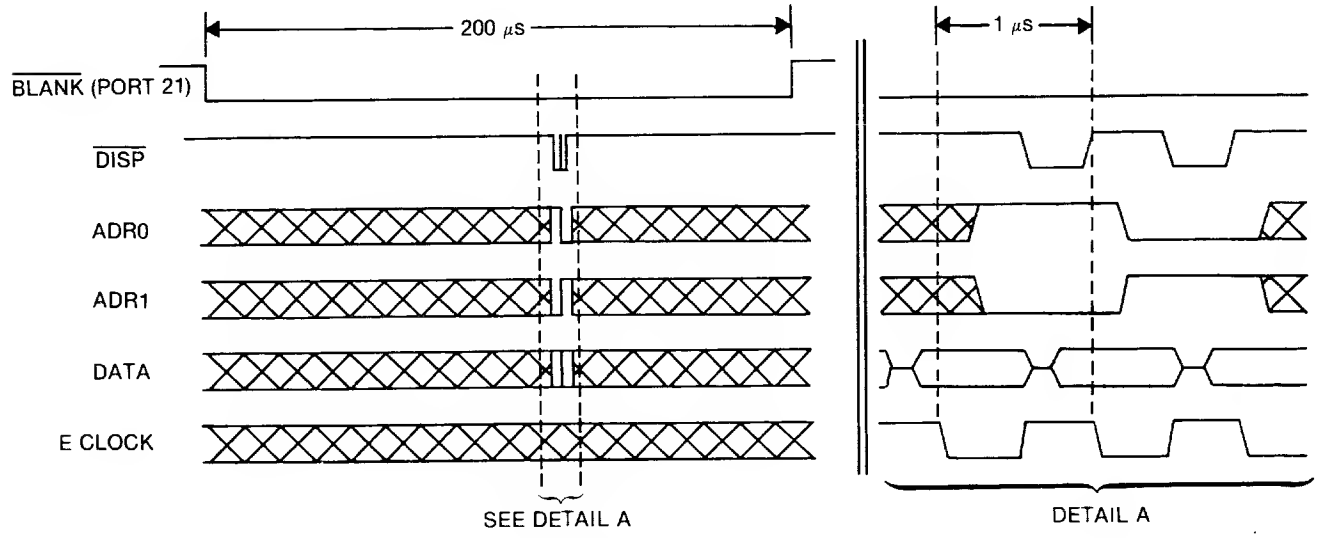


Figure 4-8. Display Segment Timing

segment drivers U1 and U2. The display segment timing is shown in figure 4-8. About 120μs after the falling edge of the BLANK, the processor loads the two-byte segment data into the segment driver registers. DISP from the address decoder strobes the buffered data (DATA0-DATA7) into U1 (lower order byte) or U2 (upper order byte) determined by ADR0 and ADR1. The rising edge of BLANK then enables the output lines (ANOA-ANO0 and ANODP) to drive the segment anodes of the display.

In the vacuum fluorescent display, all segment lines are common and individual grids enable each digit. Display filament power is provided by the driver circuit which is an IC timer, U8, configured as a 50 kHz oscillator with a 40% duty cycle. Since the output at U8 pin 3 swings from 0 to +15V, the average dc level is about +6V. This allows the grid lines to pull 6V negative with respect to the filament, which also serves as the cathode. Capacitor C14 acts as an ac ground to maintain a constant dc level across the entire length of the filament.

4.3.2 Keyboard

The keyboard section of the operator interface consists of not only the keyboard itself, (a 45 switch array mounted just behind the front panel overlay), and the keyboard decoder, U6 and U7, mounted on the display board.

The keyboard is an X-Y matrix of switches. Scanning pulses are applied to the columns of the matrix by U7, and key closures are detected at the matrix rows by U6.

Every 20 ms, the processor scans the keyboard decoder as a series of memory locations. A 4-to-10 line decoder, U7, decodes the four low-order latched address bits (ADR0-ADR3) to the 9-line side of the 9 by 5 switch array. If the operator presses a key on the front panel, the closed contact allows the appropriate decoded address line from the inverting output of the 4-to-10 line decoder (U7) to pull down 1 of 5 pull-up resistors in R3. During the data valid part of the E-clock cycle of the processor, KYBD from the address decoder enables the tri-state buffer, U6, and the processor reads a low at 1 of 5 bits on the address/data bus. The processor can then call the appropriate routine for the key pressed. If the keyboard scan finds no key pressed, the processor returns to its normal routines.

4.4 FUNCTION GENERATOR CIRCUIT DESCRIPTION

The function generator circuit board is accessible beneath the top cover of the instrument below the swing-up auxiliary board. This section includes the VCG and trigger level circuits, the basic generator loop, frequency range switches, capacitance multiplier, frequency compensation circuits, sync output driver, trigger circuit with mode logic, function select circuit including the sine converter and square logic, X-Y multiplier, preamplifier, offset amplifier, output amplifier and output protection circuits.

Refer to the function generator schematic in the back of this manual for circuits described in the following paragraphs.

4.4.1 VCG and Trigger Level

The VCG circuit converts a 0 to +10V control voltage from either the microprocessor board or the external VCG input to positive and negative currents that control the frequency of the generator loop. The input stage acts as a summing amplifier. The control voltage from the processor board, FRQ (normally between +1 and +10V), develops a current through R4 and R5 into the summing node, pin 2 of U2A. R4 and R5, with C1, also act as a filter for the FRQ line to reduce microprocessor switching noise. The first stage has a gain of approximately −0.4, so its output at U2A pin 1 ranges typically −0.4V to −4.0V. When the external VCG input is used, FRQ is normally set to 0V by programming FREQ 0, EXEC from the front panel, and the voltage from the external VCG input across R6 now determines the first stage output. CR1 and CR2 prevent excessive voltage at VCG IN from damaging the VCG amplifier. For frequencies between 10 MHz and 12 MHz, an overrange control, $\overline{OVR}$, adds a fixed 0.2 mA through R1 and R2 to increase the maximum voltage out of the first stage (or current out of the entire VCG circuit). The 10 kHz to 99.9 kHz range control, $\overline{FR5}$, increases the current from FRQ by paralleling R3 across the series combination of R4 and R5. This increase compensates for the larger relative capacitance on this range due to the minimum triangle node capacitance (C43 and C44) added to the smallest fixed range capacitor (C50). A gain adjustment (R8) in the first stage is used to control the top-of-range frequency. R11 controls the first stage offset to zero the low end of the external VCG input.

The output of the VCG Amplifier, VCGO, is routed to the auxiliary board where it is summed with the output of the phase-locking circuits. This modified voltage returns to the function generator board on the VCGI line. With the VCG JUMPER in its normal operating position (E10 to E11), this VCGI voltage becomes the VCV (Voltage Control Voltage) output to the variable current sources and the high-frequency compensation circuit. In the Wavetek 278, the E9 to E10 connection of the VCG JUMPER is used only for disconnecting the synthesizer board output during calibration. A simplified schematic of the VCG amplifier is shown in Figure 4-9.

The current sources operate on the following principles:

1. The collector current of a transistor depends on its base current and its current gain, and is relatively independent of collector load resistance.
2. The base drive of a transistor can be adjusted to provide a known reference current in its collector circuit.
3. This same base drive, applied to a second matched transistor, will cause the second transistor to have the same collector current as the first transistor.

The negative current source is shown in Figure 4-10 simplified schematic diagram. The Voltage Control Voltage (VCV) is inverted by operational amplifier U2C, and drives transistor U3A to whatever value collector current is required to cause the U3A collector voltage to be equal to VCV. (At this point, both inputs of operational amplifier U2C are at the same voltage,

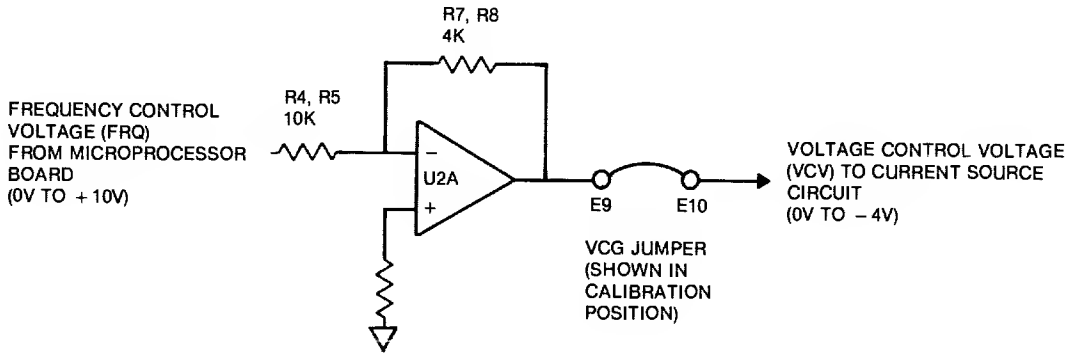


Figure 4-9. Simplified Schematic Diagram, VCG Amplifier

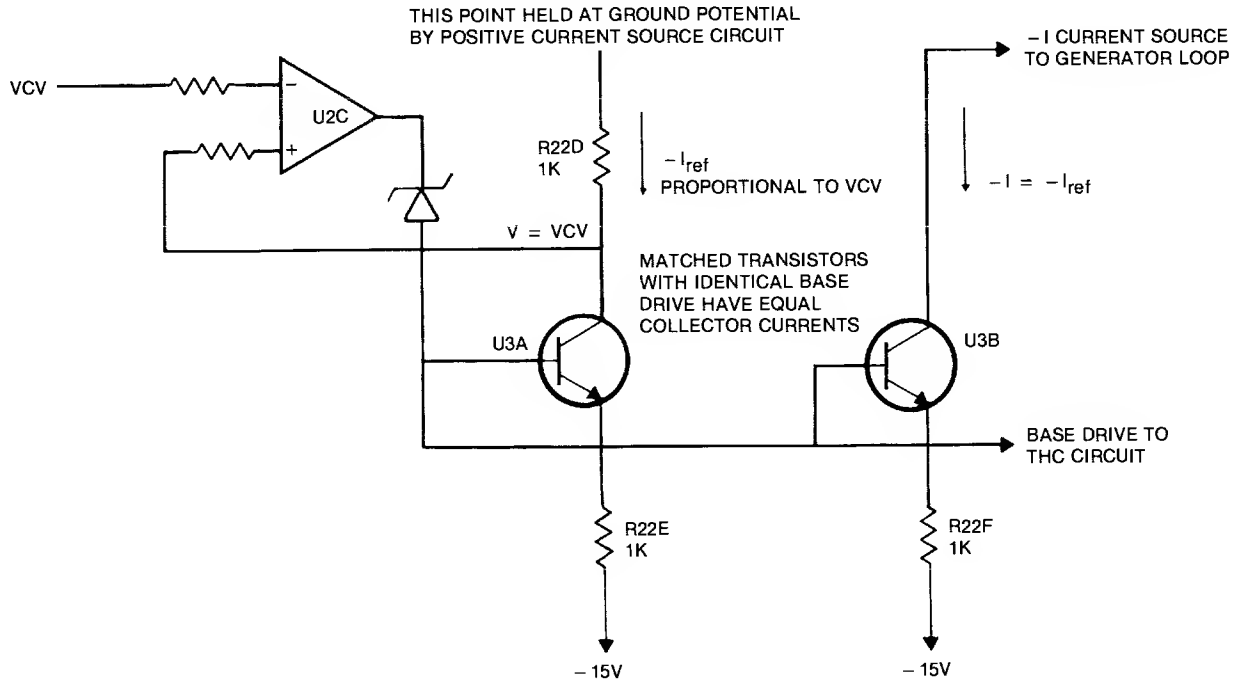


Figure 4-10. Simplified Schematic Diagram, Negative Current Source

and equilibrium is established.) Since the upper end of collector resistor R22D is held at ground potential (as will be explained later) and the voltage at the lower end is equal to VCV, the current through the resistor ($-I_{ref}$) is proportional to VCV. The same base drive is applied to U3B to generate the negative current source (−I), and is also applied to transistors U3C and Q1 to generate the Trigger Holding Current (THC).

The positive current source (shown in simplified schematic Figure 4-11) operates in a similar manner, and tracks the negative current source. Operational amplifier U2D drives transistor U3E to whatever value collector current is required to maintain a "virtual ground" at the junction of R22C and R22D. Since these two resistors are in series, their currents are equal ($+I_{ref} = -I_{ref}$). The U3E base drive is then applied to matched transistor U3D to generate the positive current source (+I) for the generator loop.

The current source circuit also generates a Trigger Holding Current (THC) which is used to clamp the triangle node at ground potential during the "off" state in the gated and triggered modes. The circuit is shown in simplified schematic diagram Figure 4-12.

The same transistor base drive that creates the negative current source (−I) is also applied to transistors U3C and Q1, driving each transistor to a collector current equal to −I. The two collectors are connected in parallel to provide a current equal to twice the −I current source. This −2I current is supplied by CR14 in the trigger circuit while the generator is gated "on".

When the generator is gated "off", a negative voltage is applied to the CR14 anode. This transition always occurs at the negative peak of the triangle waveform, and the −2I current is momentarily supplied by CR7. As the triangle node rises toward ground potential, a greater proportion of the −2I current flows through CR8. Equilibrium is reached when the trigger holding current is equal to the positive current (+I) being supplied to the generator loop, and the triangle node voltage cannot rise any further. Since matched diodes CR7 and CR8 have equal currents through them and the anode of CR7 is grounded, the voltage drops across the two diodes will also be equal and the triangle node will be held at ground potential. This stops the waveform smoothly at the leading edge and ensures that at least one complete cycle will be generated every time the generator is triggered.

R23 adjusts the positive current source to precisely match the negative current and therefore maintain waveform symmetry. R12, which adjusts the low end

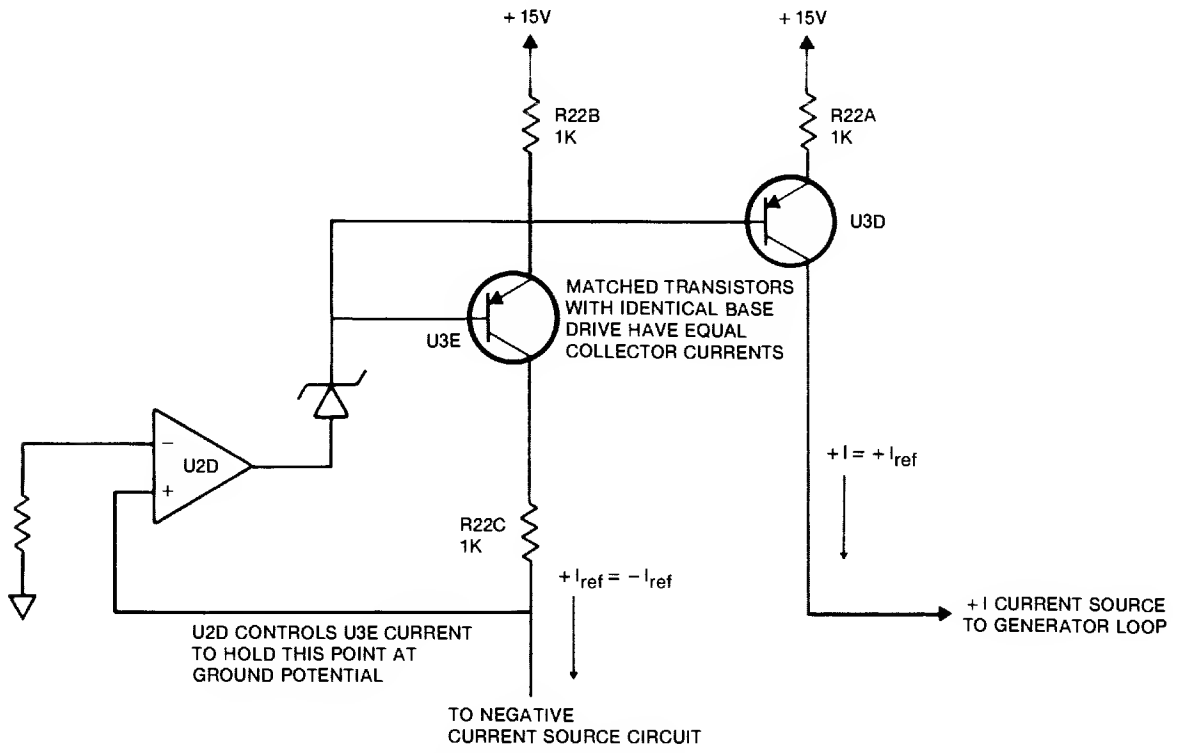


Figure 4-11. Simplified Schematic Diagram, Positive Current Source

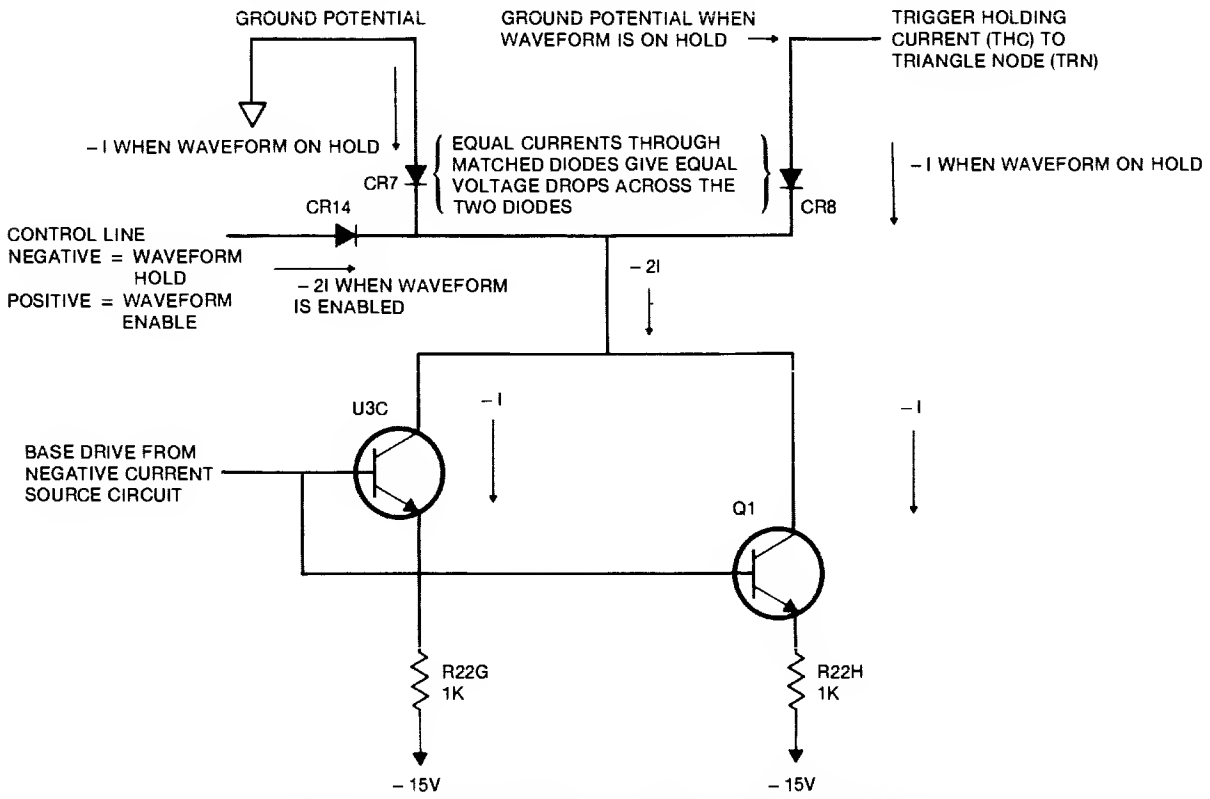


Figure 4-12. Simplified Schematic Diagram, THC Circuit

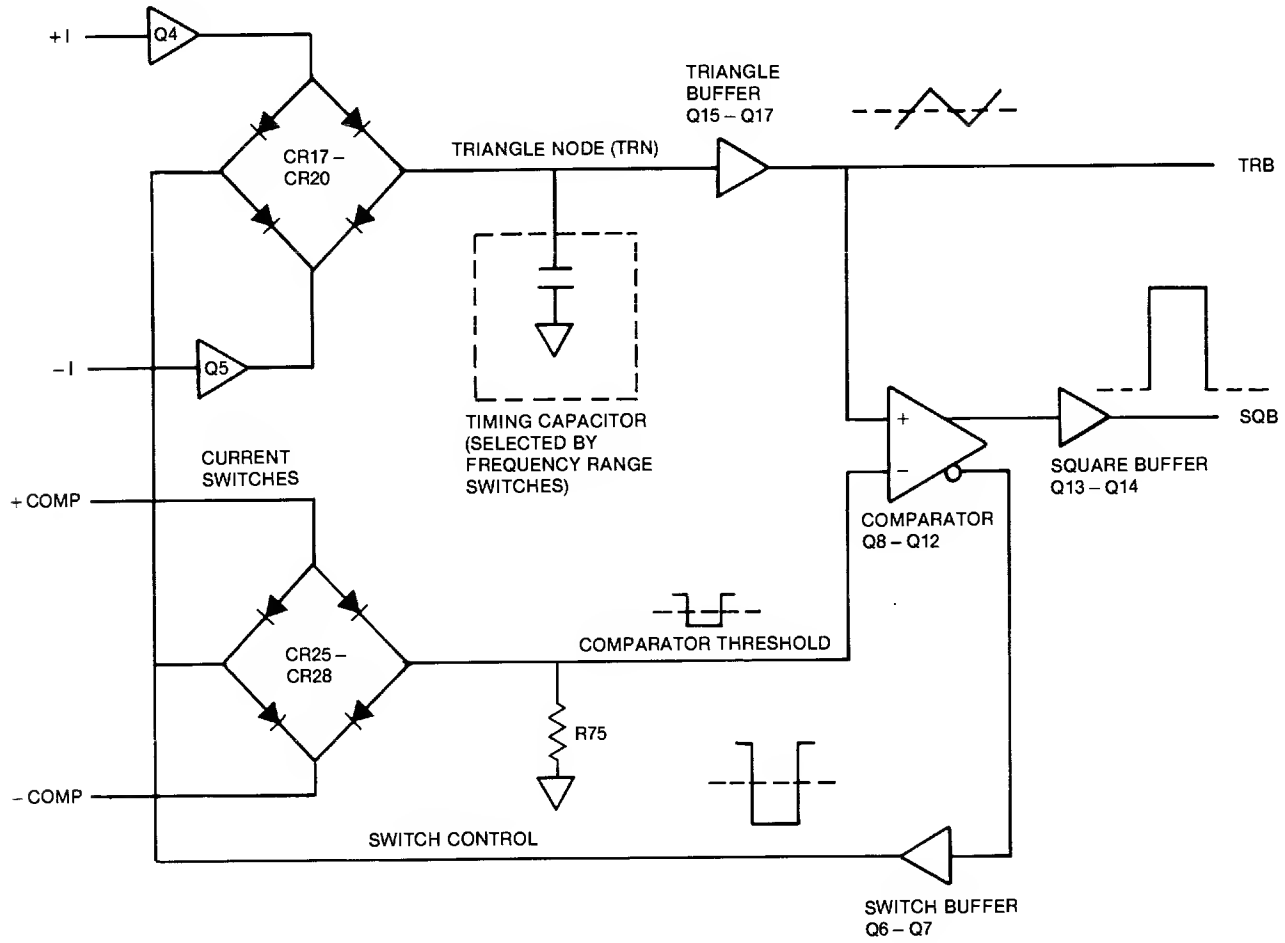


Figure 4-13. Simplified Schematic Diagram, Generator Loop

frequency, sets the offset of the positive current amplifier, U2D to match the offset of the negative current amplifier, U2C. R15 adds or subtracts current through the reference string to balance symmetry at low currents. The 8.2V zener diodes, CR4 and CR6, allow U3 pins 14 and 1 to approach the positive and negative supply rails respectively. Diodes CR3 and CR5 prevent latch-up.

The trigger level amplifier consists of an operational amplifier (U2B) in an inverting configuration that translates the trigger level control voltage from the microprocessor board (TRL, 0 to +10V) to the level used at the trigger comparator (TLO, +10V to −10V).

4.4.2 Generator Loop

The Generator Loop, shown in simplified schematic diagram Figure 4-13, produces simultaneous square and triangular waveforms. The triangular waveform is generated by alternately charging and discharging a timing capacitor from adjustable constant-current sources. The value of the selected timing capacitor determines the frequency range of the loop. Within any range, frequency is determined by the magnitude of the +I and −I currents from the VCG circuit. Charging the capacitor from a current source gives a linear voltage change with respect to time, instead of the exponential curve that would result if a resistor were used.

The comparator monitors the amplitude of the triangle wave, and when it reaches the comparator threshold, the comparator changes states. The state of the comparator output determines the polarity of the comparator threshold and the direction of the capacitor charge/discharge current. The comparator output is also used to generate the square wave output.

Magnitude of the comparator threshold is determined by the value of the +COMP and −COMP currents from the high frequency compensation circuit. The positive or negative current selected by current switch CR25-CR28 flows through R75, and the voltage

drop across R75 becomes the comparator threshold voltage. The high frequency compensation circuit reduces the +COMP and −COMP currents on the three highest frequency ranges to reduce the comparator threshold voltage to compensate for switching delays.

Operation of the diode current switch is illustrated in simplified schematic diagram Figure 4-14. In this simplified schematic, voltage drops across the forward-biased diodes are assumed to be 0.6 volts, and the voltages shown are not intended to represent **exact** circuit voltages. Although this diagram shows the CR17-CR20 current switch, the same principles of operation also apply to the CR25-CR28 circuit.

The current switch has three inputs and one output. The inputs are the positive and negative currents (buffered by Q4 and Q5) and the control voltage; the output is the switched current. The magnitude of the control voltage must be greater than the voltage at the output that is caused by the switched current flowing through the external load. In this example, voltage at the triangle node (TRN) will not exceed ±1V before the comparator changes states and causes the voltage to move in the opposite direction.

With the control input at +2V, CR18 and CR19 are reverse biased. Current flows from the +I source through CR17 into the timing capacitor, and from the control line through CR20 into the negative current source. With the control line input at −2V, CR17 and CR20 are reverse biased. Current flow is from the +I source through CR18 into the control line, and from the timing capacitor through CR19 to the −I source.

The CR25-CR28 current switch operates in a similar manner. Voltage at the output of this switch is limited to ±1V by the 3 mA maximum value of the current and the 332 ohm resistance of R75.

For the remainder of the circuit description of the Generator Loop, refer to the complete schematic diagram.

The comparator is made up of current source Q10, differential pair Q9 and Q11, and a second differential pair, Q8 and Q12. As the rising ramp of the triangle wave at the base of Q11 reaches the positive reference level (+1V) at the base of Q9, Q11 of the differential pair turns on as Q9 turns off. CR29 and CR30 increase the transistor switching speed by limiting the signal swing at the collectors of Q9 and Q11 to about

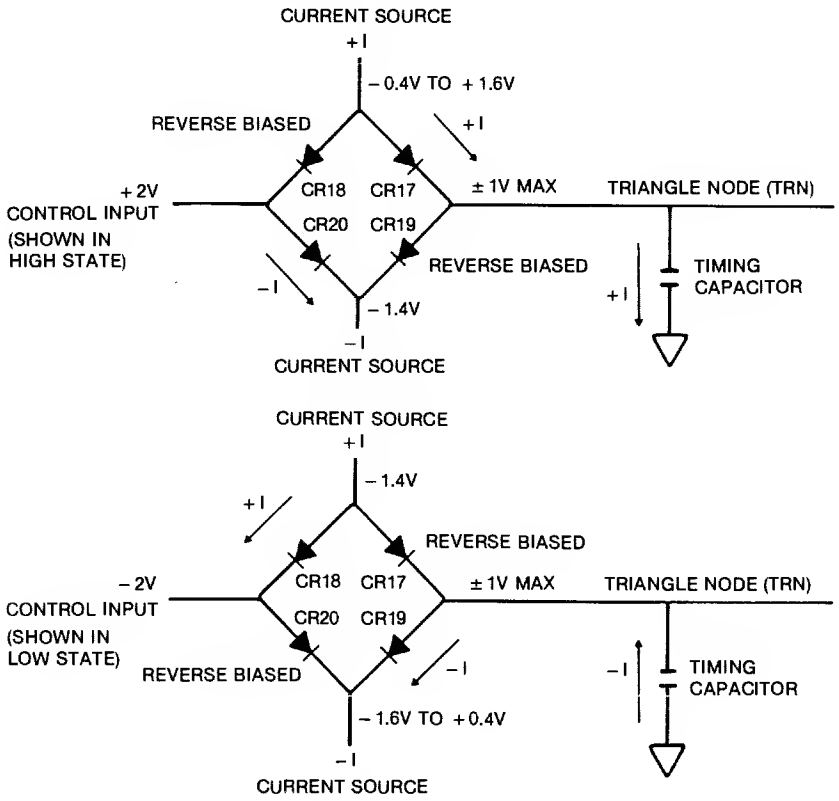


Figure 4-14. Simplified Schematic Diagram, Current Switch

0.7V. As Q9 and Q11 switch, they also cause the second differential pair, Q8 and Q12 to switch. Resistors R72 and R84 increase the switching speed of Q8 and Q12 respectively by providing a small current which keeps them from turning entirely off. As Q8 switches to its relatively "off" state, current through R73 decreases and the collector of Q8 falls to its low state, about −1.6V, determined by the current drain through R71. The collector of Q8 drives the switch buffer; the square buffer is driven by Q12 in the opposite side of the comparator. These two stages have different values of collector and emitter resistors to match the output requirements of the associated buffers.

The switch buffer (Q6-Q7) is a push-pull emitter follower biased on by the voltage drops across CR22 and CR23. The output is a ±2.2V square wave that drives the two current switches in the generator loop.

The square buffer (Q13-Q14) is similar to the switch buffer circuit, except that resistor values are tailored for a 0 to +5V output. This signal, SQB, is used to drive the sync driver and trigger circuits. The SQB signal is attenuated by R100 and R101 to provide the SQS signal used by the square logic and the auxiliary board. A highly differentiated portion of the SQB transient is coupled through C35, C36 and C27 to the triangle node to counteract switching transients which are coupled through the current switch diode bridge.

The alternating linear ramp (triangle wave) at the triangle node is buffered by the triangle buffer, a high speed FET input voltage follower. This circuit consists of Q15, acting as a source follower, and Q16, acting as an emitter follower. The voltage difference between the input and output of the circuit is controlled by maintaining the current through Q15 so that the gate-source voltage is equal and opposite to the base-emitter drop of Q16 and the two voltages cancel each other. The current through Q15 is initially set by adjusting R99, the NODE DC adjustment, after which the dc amplifier in the frequency compensation circuit maintains this adjustment through the constant current source, Q17, to compensate for temperature changes in Q15.

4.4.3 Frequency Range Switches

The selected range capacitor determines the frequency range from 100 Hz to 12 MHz. Each range normally covers 10% to 99.9% of full scale. Capacitance for the highest frequency range consists of all the stray capacitance on the triangle node added to C43 (the 1 MHz adjustment capacitor) and C44, which brings the total to 100 pF. The next range switches in an additional 900 pF, made up of C46, C47 and the 100 kHz adjustment C45. The next three ranges switch in successive matched capacitors of 0.01 μF (C50), 0.1 μF (C52) and 1.0 μF (C54).

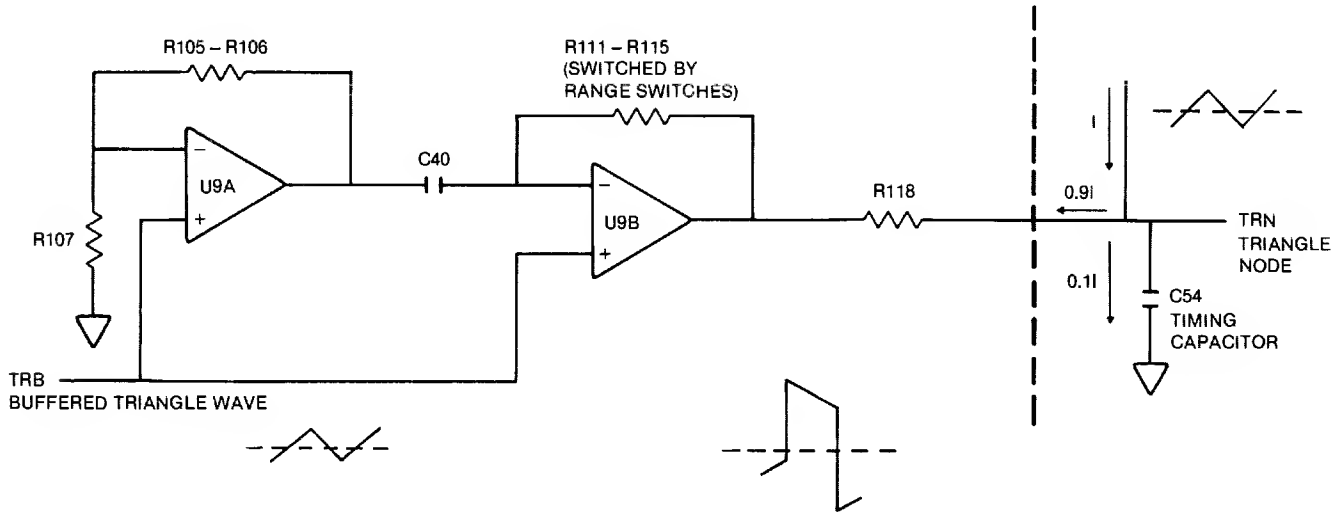
Each range capacitor is switched in by a logic level signal from the microprocessor board. For example, When $\overline{FR6}$ (Frequency Range from 0.1 MHz to 1 MHz) goes low, it turns on Q18, which sources about 30 mA through R124 and diodes CR36 and CR37. When CR37 is forward biased with this amount of current, its impedance to ground is less than 2Ω, and the range capacitor made up of C45, C46 and C47 is effectively connected to ground. When this range is not selected, $\overline{FR6}$ is high, turning off Q18 and allowing R125 to pull the anode of CR36 to −15V. The voltage divider, R121 and R122, pulls the anode of CR37 to −7.5V through the 10MΩ resistor R123. Reverse-biased CR37 now provides an essentially infinite impedance, effectively disconnecting the range capacitor. The other range switches operate in exactly the same way.

4.4.4 Capacitance Multiplier

The capacitance multiplier extends the low end frequency range by drawing off (through R118) most of the charging current to and from the largest range capacitor, C54. The circuit is shown in simplified form in Figure 4-15. The U9B output waveform is a triangle wave superimposed on a square wave. The square wave component determines the polarity of the voltage across R118, and therefore the **direction** of current flow through this resistor. The triangle component maintains the **magnitude** of the R118 voltage and current constant to maintain linearity of the triangle node waveform.

The square wave component is generated by differentiating the triangle wave. The triangle wave is amplified by U9A, then differentiated by C40 and U9B. U9B also sums the triangle wave at its non-inverting input with the square wave. The resulting output is applied to the triangle node through R118.

The capacitance multiplier is switched in at frequencies below 100 Hz by a logic low on the $\overline{CPM}$ control line. The proportion of capacitor charging current is determined by the range resistors. $\overline{FR2}$ selects R111 (plus the 99.9 Hz adjust, R112) and decreases the capacitor charging current to 10% of its normal value. Each successive decade of added resistance decreases the capacitor current to 10% of its previous range. R105 adjusts the overall calibration of the capacitance multiplier by adjusting the gain of the first amplifier, and R117 adjusts the capacitance multiplier symmetry by adjusting the offset of the second amplifier.



NOTES:

1. Direction of currents shown is for capacitor charging in positive direction.
2. Ratio of capacitor current to total current depends on frequency range selected.

Figure 4-15. Simplified Schematic Diagram, Capacitance Multiplier

4.4.5 Frequency Compensation

The Frequency Compensation circuit contains the high frequency compensation, which reduces the Generator Loop comparator threshold on the three highest frequency ranges to compensate for comparator switching delays, and the dc amplifier circuit, which dynamically controls the dc offset in the triangle buffer.

The high frequency compensation circuit is shown in simplified schematic diagram Figure 4-16. This circuit generates the two adjustable constant currents (+COMP and −COMP) that alternately flow through R75 in the comparator circuit in the Generator Loop to develop the comparator threshold voltages. On the lower frequency ranges, these currents each have a fixed value of 3 mA. On the three highest ranges, the currents are reduced in proportion to both the range selected and the programmed frequency within the range.

On the lower frequency ranges, the range switches are all open, and voltage divider R53, R50, R52 develops a voltage of +7.5V at the junction of R53 and R50. This voltage is applied to the non-inverting input of operational amplifier U7B, which drives the source of Q2 (and the inverting input of U7B) to the same voltage. The resulting +7.5V at the junction of R56 and R54 causes a current of 3.75 mA in R56 and 0.75 mA in R54. The difference of these two currents is the 3 mA +COMP current.

U7A and Q3 track the positive current source to generate a negative current (−COMP) of equal magnitude. U7A monitors the voltage at the midpoint of R54 and R57, which are connected in series between the source of Q2 and the source of Q3. As U7A acts to keep its two inputs at equal voltage (and the midpoint of the resistors at ground potential) it drives the Q3 source to a voltage equal in magnitude and opposite in polarity to the voltage at the Q2 source. The Q3 source voltage determines the currents in R57 and the series combination of R59 and R60. The difference of these two currents is the 3 mA −COMP current.

Operational amplifier U7C converts the negative Voltage Control Voltage (VCV) to a voltage that is positive in proportion (within any frequency range) to the programmed frequency. Although the range of this voltage is 0V to +6V, it will normally be above +0.6V except at the bottom end of the lowest frequency range. On the top three frequency ranges, one of the solid-state range switches is closed by a logic low on its control line, connecting this voltage through one of the range resistors (R42, R43 or R47) to the R53, R50, R52 voltage divider. This raises the voltage at the junction of R53 and R50, causing the absolute values of the Q2 and Q3 source voltages to increase and the source currents to decrease. The result is a decrease in the +COMP and −COMP currents proportional to both frequency range and programmed frequency within the range.

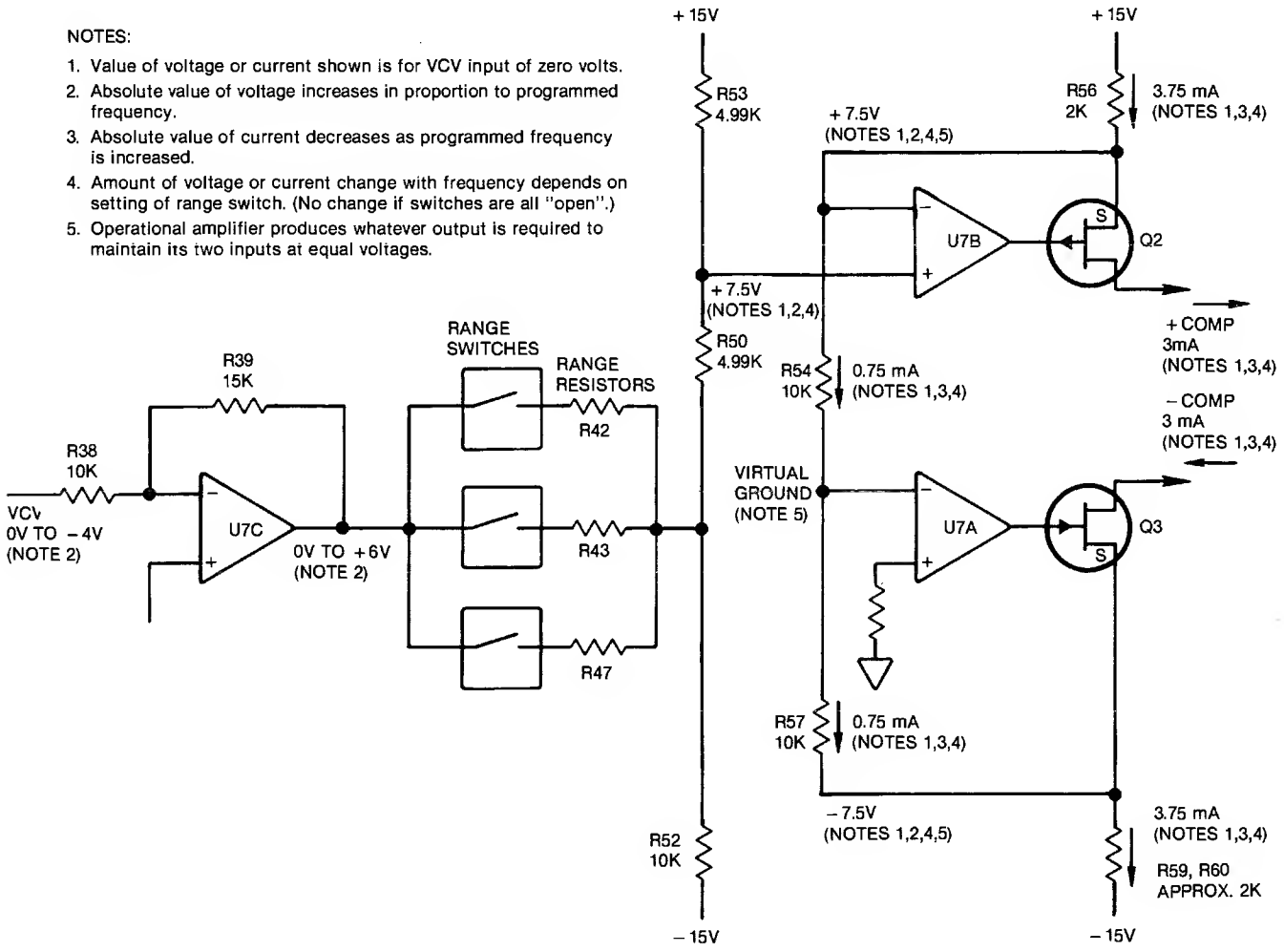


Figure 4-16. Simplified Schematic Diagram, High Frequency Compensation

R44 causes a small voltage change in the output currents proportional to VCV to compensate for a small non-linearity in frequency tracking. R60 balances the triangle waveform, while R45 and R46 allow adjustment of frequency on the top two frequency ranges. Zener diodes CR15 and CR16 (not shown on the simplified schematic) act as level shifters to allow the operational amplifier outputs to operate near ground potential while the gates of Q2 and Q3 operate closer to the supply voltages.

The dc amplifier keeps the output of the triangle buffer at the same dc level as the input by varying the current through the constant current source, Q17, and therefore through the input FET, Q15. It does this by comparing highly filtered signals at the operational amplifier inputs, U7D pins 12 and 13, and varying the current through R104 to compensate for errors. Below 100 Hz, $\overline{\text{DCA}}$ switches out filter capacitors C17 and C58; this allows amplifier U7D pin 14 direct control of the current through R104, thus giving greater accuracy.

4.4.6 Sync Driver

The Sync Driver is a double emitter follower that buffers the generator loop's square output, SQB, to provide a synchronizing signal for the instrument.

Transistors Q26 and Q27 are biased on by the voltage drop across CR52 and CR53. R171 and R175 provide about 4 mA through the diodes, and resistors R173, R181 and R183 balance the current so the transistors also have about 4 mA through them. The small emitter resistors also prevent thermal runaway. Collector resistors protect the transistors from overvoltage at the output connector, and capacitors C70 and C71 prevent large signal swings at high frequencies that would reduce the gain of the transistors and add noise to the circuit.

4.4.7 Trigger Circuit

The trigger circuit allows the instrument user to trigger or gate the generator from an external signal of widely varying characteristics with a fixed and stable delay between the trigger source and the resultant generator output.

Trigge, comparator U4 compares the level of the trigger inpu' with the reference level (TLO) programmed in the generator. The comparator output goes to a logic low at U4 pin 9 if the trigger input becomes greater than the reference level and positive trigger slope (+TR) has been selected, or it goes to a logic low at U4 pin 11 if the trigger input becomes less than the reference level and negative trigge, slope (−TR) has been programmed. A logic low transition at either comparator output will cause a logic high at the pin 8 output of NAND gate U5C; this positive-going transition clocks the remainder of the trigger logic.

In the Wavetek 278, the output of the trigger comparator at U5C is always routed through the auxiliary board, and the TRIG JUMPER is connected from E13 to E14. This jumper must **never** be connected from E12 to E13, as this will place the output of NAND gate U5C on the function generator board in parallel with the output of U8C on the auxiliary board.

Refer to Figure 4-17, Simplified Schematic Diagram, Trigger Circuit Mode Logic, for the following discussion. The trigger circuit is enabled by a logic high on the MC0 line. Selection of triggered or gated mode is performed by logic line MC1; the line is low for triggered mode or high for gated mode.

In the triggered mode, only one cycle of generator output is enabled for each trigger pulse applied. A logic low on mode control line MC1 disables NAND gate U5D. The high level on the output of U5D disables the direct $\overline{SET}$ input of flip-flop U6B and enables NAND gate U5B. A positive logic transition at trigger jumper terminal E13 clocks flip-flop U6B to the "set" condition, causing the $\overline{Q}$ output to go low. This low is applied to the direct $\overline{CLEAR}$ input of U6A, giving a logic low at the U6A Q output. The low at U6A-Q causes a high at the output of NAND gate U5A, reverse biasing diode CR8 and allowing the generator loop to oscillate. The first positive transition of SQB, 90° later on the triangle waveform, is inverted by NAND gate U5B and applied to the $\overline{CLEAR}$ input of U6B to clear the Q output high, thereby removing the low from the $\overline{CLEAR}$ input of U6A. The next negative transition of SQB is inverted by U5B, and clocks U6A to the "set" condition. The high at U6A-Q causes the output of gate U5A to go low, forward biasing diode CR8 and stopping the triangle oscillation on its rising edge.

In the gated mode, the generator output is continuously enabled for the entire duration of the applied tigger signal. A logic high on mode control line MC1 enables NAND gate U5D, causing the U5D output to be low whenever the E13 trigger level is high. Operation in the gated mode is the same as in the triggered mode except that during the time that the E13 trigger level is high, the resulting low at the U5D output will:

1. Hold flip-flop U6B in the "set" condition via the direct $\overline{SET}$ input.
2. Disable NAND gate U5B, preventing the SQB signal from clearing U6B and clocking U6A until after the trigger signal is removed.

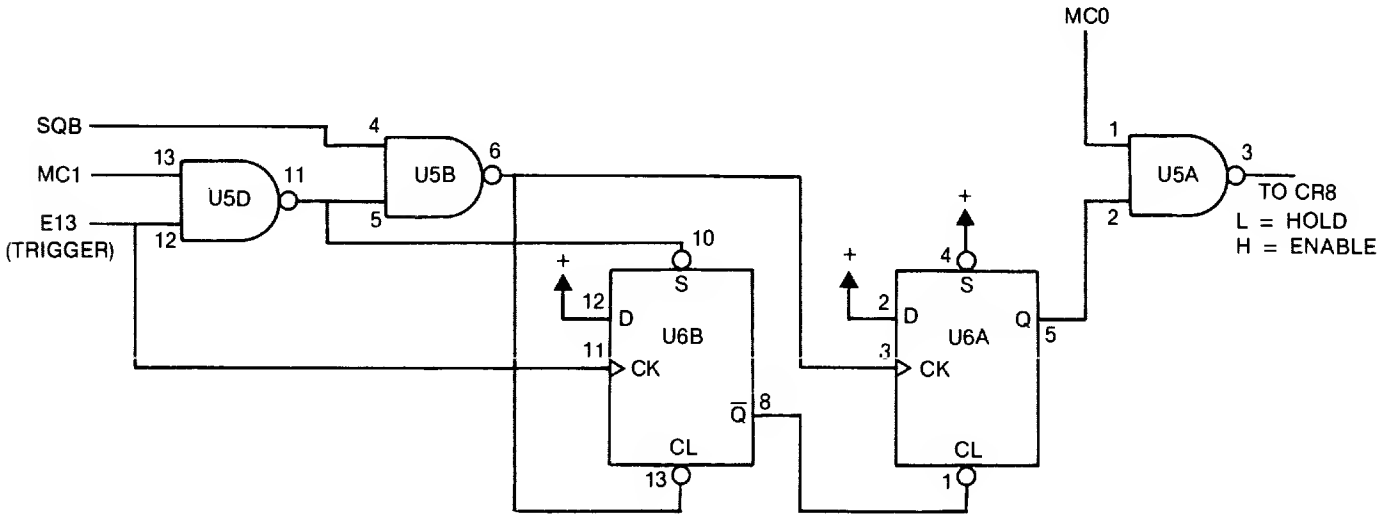


Figure 4-17. Simplified Trigger Circuit Mode Logic Schematic Diagram

Resistors R29, R303, R34, R31 and R32 divide the reference (TLO) and input (TRIG IN) voltages by a factor of 4 to bring them within range of the U4 comparator. Diodes CR9, CR10 and CR11 protect the U4 comparator from excessive voltage at the trigger input. Resistors R33 and R35 provide a small amount of hysteresis at the U4 comparator input to prevent false triggering on noise.

4.4.8 Function Select

The function select circuit connects the sine, triangle or square (all disconnected in dc) to the current input of the X-Y multiplier.

The sine wave input is created from the triangle buffer output, TRB, by the sine converter which uses the logarithmic response characteristics of semiconductor diodes to approximate a sine wave current output. The SIN DIST A adjustment, R142, adjusts the converter input for diode forward voltage variation. The six diodes in U11 give a three stage sine approximation using the very closely matched characteristics of the diodes. Two adjustments, SIN DIST B and C (R154 and R157), balance between stages for positive and negative peaks respectively. The current output is switched through FET switch U12A when SIN is selected.

The triangle level control (R148) provides an adjustable current to FET switch, U12C, controlled by TRI. Both the triangle and sine FET switches provide increased isolation by shorting the FET switch input to ground (with Q25 and Q22 respectively) when the switch is off.

The square logic selects which square waveform is fed to the square shaper. A logic high on the SQR control line selects the univerted SQS square wave, while a high on the SQR line selects the SQS signal after it has been inverted by U13C. A logic high on the external width control line (EXW) selects the output of the trigger circuit, TRGI.

The pulse input PLSI, and associated control lines PLS and $\overline{\text{PLS}}$ are not used in the Wavetek 278. The Wavetek 278 generates repetitive pulses by internally triggering the function generator from the internal synthesizer output. The microprocessor converts entries for period and width into synthesizer and function generator frequencies, and also converts the settings for upper and lower pulse levels into amplitude and offset.

The square shaper converts the TTL level signal at U13A pin 3 to ± 1 mA. It shifts the TTL signal and uses it to switch current sources through a diode switch (CR48 through CR51) and into the FET switch U12D (controlled by $\overline{\text{RCT}}$). The current sources for upper and lower levels of square waves are independently adjustable by R164 and R168 respectively.

4.4.9 X-Y Multiplier and Offset

4.4.9.1 X-Y Multiplier

The X-Y multiplier is a precision voltage-controlled amplifier that drives the preamplifier with a signal level directly proportional to the amplitude control voltage (AMP) from the microprocessor board.

As shown in Figure 4-18 block diagram, the X-Y multiplier consists of five major circuit groups: logarithmic signal compressor, variable gain signal amplifier, logarithmic dc reference, variable gain reference amplifier, and dc amplifiers. The input signal (XYI) is logarithmically compressed in U18A, then amplified by variable gain signal amplifier U19A. Because the control voltage versus gain characteristic of the variable gain amplifier is not linear, the remainder of the circuit is required to convert the input amplitude control voltage (AMP) to a modified gain control voltage.

U18B generates a dc reference voltage proportional to the logarithm of the difference of two currents. This reference voltage is amplified by variable gain reference amplifier U19B and fixed gain dc amplifiers U17A and U17D, then compared to the amplitude control voltage (AMP) by U17B. U17B provides the modified gain control voltage to both variable gain amplifiers, and adjusts the gain of the reference amplifier upwards or downwards as required until the amplified reference voltage is equal to the input amplitude control voltage (AMP). The same modified gain control voltage that controls the gain of the variable gain reference amplifier is also applied to the variable gain signal amplifier.

The logarithmic signal compressor (U18A) consists of a differential transistor pair connected as diodes. One side of the differential pair is connected to ground, the other side to the XYI signal line. Each side of the differential pair is biased to about 3 mA (the optimum diode current for logarithmic compression) by the current source transistor within the IC. The input signal current (± 1 mA) on the XYI line causes a small ac voltage across the diode that varies approximately as the logarithm of the total current. This voltage also drives one base of the output differential pair (U19 pin 2), while the other base is approximately at ground potential, adjusted by the multiplier distortion adjustment, R255. The current source transistor in the output stage (U19 pin 3) is driven by the modified gain control voltage. Maximum output from the stage

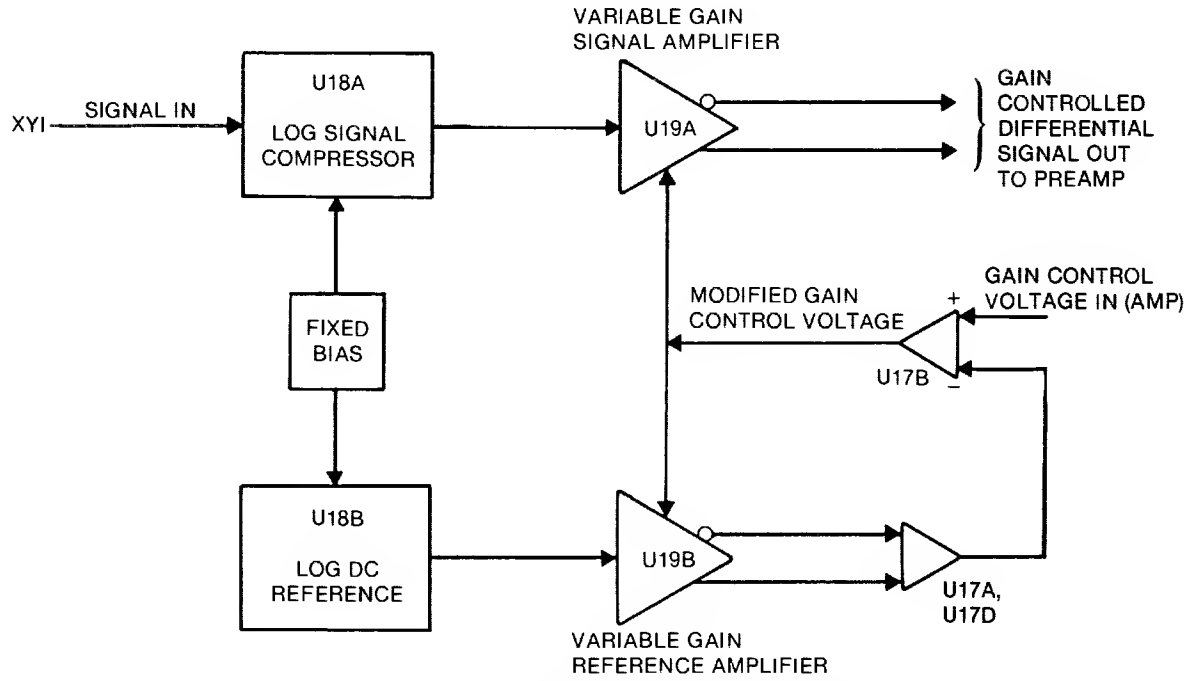


Figure 4-18. X-Y Multiplier Block Diagram

occurs with a maximum total bias current of 6 mA; less bias current produces less output.

The logarithmic dc reference (U18B) is configured much the same as the logarithmic signal compressor, as described above. Total bias current through the differential pair is fixed at 6 mA, but unevenly split with 4 mA through one side and 2 mA through the other side (limited by R242 and R243). This corresponds to the current ratio in the signal compressor during peaks of the signal, when the instantaneous peak signal current of 1 mA adds to the 3 mA dc current in one half of the differential pair and subtracts from the 3 mA dc current in the other half. The dc reference voltage is taken from U18 base and collector terminals 8 and 9.

A simplified schematic diagram of the variable gain reference amplifier and associated dc amplifiers is shown in Figure 4-19. The input amplitude control voltage (AMP) drives U17B (pin 5), which in turn drives the base (pin 11) of the current source transistor in U19B. The base of one side of the differential pair (U19 pin 9) is connected to ground through a resistor; the base of the other side of the pair (U19 pin 6) is connected to the log dc reference voltage. These base voltages will maintain the currents in the differential pair in the ratio 1:2 regardless of total current flow determined by the current source transistor. The collectors of the differential pair are connected to the inverting inputs of operational amplifiers U17D and U17A (pins 13 and 2). These inverting inputs are "virtual grounds"; because the non-inverting inputs of these amplifiers are grounded, each amplifier will provide whatever output level is required to keep its two inputs at the same voltage level. The value of resistors R256 through R258 were chosen so that with 6 mA through the current source transistor in U19B:

1. 2 mA flows through R256 from U17D pin 14 to U19B pin 7.
2. 2 mA flows through R257 from U17D pin 14 to U19B pin 8.
3. An additional 2 mA flows from U17A pin 1 through R258 to U19B pin 8.
4. The voltage at the output of U17A (pin 1) is 10 Vdc, which exactly equals the 10 Vdc external AMP input, maintaining the inputs of U17B (pins 5 and 6) at equal voltages.

With input amplitude control voltage (AMP) less than 10V, all voltages and currents in the circuit are proportionately less.

The output of the circuit is the modified gain control voltage at the output of U17B (pin 7). This voltage is used to control the variable gain signal amplifier.

Fixed bias for both sections of U18 is provided by R248, CR59 and CR60. CR61 performs a level shifting

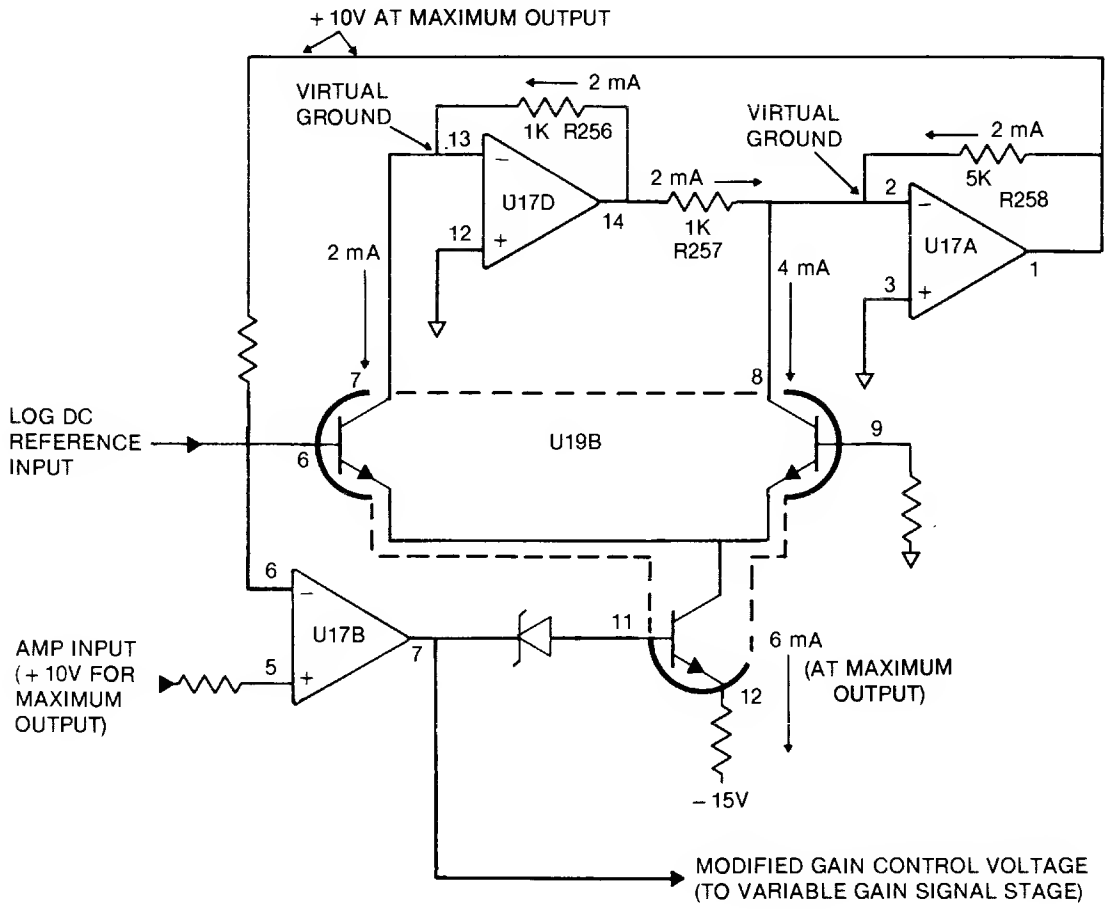


Figure 4-19. Variable Gain Reference Amplifier

function, allowing the base terminals of U19 (pins 3 and 11) to operate near the negative supply voltage while the output of U17 (pin 7) operates closer to ground potential.

The X-Y multiplier circuit contains four calibration adjustments: R241, R242, R251 and R255. Adjustment procedure for these controls is given in the CALIBRATON section of the manual.

4.4.9.2 Offset Circuit

The offset circuit is a level translator that converts the 0 to +10V input from the microprocessor board (OST) into a +5 to −5 Vdc signal that is sums into the output amplifier. Any offset caused by the operational amplifier at U17C pin 8 is corrected by the offset zero adjustment, R237. The output of the amplifier is then adjusted for dc offset by the offset adjustment, R208.

4.4.10 Preamplifier

The preamplifier takes the differential current output of the X-Y multiplier from U19 pins 1 and 14 and converts it to a single-ended voltage output at the anode of CR54. The voltage at the inputs of the differential stage (U15 pins 3 and 16) must be maintained at about +0.7 volts to bias the input transistors whose emitters are at ground. The emitter of the transistor at U15 pin 8 provides the current to maintain this voltage. The current can be as high as 6 mA or as low as 0.06 mA, depending on the current required by the output stage of the X-Y multiplier. Added to this current is the bias current for the preamplifier itself, about 1 mA each through the feedback resistor strings consisting of the 750Ω, 0.1% resistors R189 and R192, and R194 and R198. The full-scale current output of the X-Y multiplier is ±1 mA in each leg of the output differential stage, and this current is translated into a ±0.75 Vac signal at U15-8 and a ±1.5 Vac signal of the opposite phase at the CR54 anode. PNP transistors Q28 and Q29 act as constant current sources for the input stage collectors (U15-2 and U15-1 respectively) and they also act as an ac

bootstrap through coupling capacitors C76 and C79. The emitter follower stages, U15-8 and U15-11, isolate the collectors of the input stages to provide a low impedance output.

4.4.11 Output Amplifier

The output amplifier is an inverting and summing amplifier with a gain of about 6.67 for the ac signal from the preamplifier. The amplifier operates differently for high-frequency signals than for low-frequency signals: high-frequency signals couple into the symmetric emitter followers Q30 and Q31 through capacitors C90 and C91 respectively. The emitter followers then drive the symmetrical inverter stage consisting of Q32 and Q33. Diodes CR55 and CR56, with the 10Ω resistor, R219, provide a bias current through the output stage of Q34, Q35, Q36 and Q37 to increase output speed by keeping the transistors always on. The 10Ω emitter resistors, R227, R228, R231 and R232, balance the current through the parallel output stage transistors to improve their power handling capability. The output signal (+ and − 10V, maximum) is fed back through resistors R223 and R217 in series to the input. The trim capacitors, C97 (output amplifier peaking) and C122 (output amplifier roll-off), adjust the amplifier high speed characteristics by rolling off or peaking the feedback signal respectively.

The low-frequency (and dc) path in the output amplifier is through the transistor array, U16, connected as an operational amplifier. The positive output of the differential input stage (U16-3) is inverted at U16-9. This signal decreases the current through transistor Q32 and the signal at its collector falls until the feedback signal balances the input, either ac (through R207) or offset (through R208 and R209). The PNP transistors in U16 balance the current through the differential input pair and provide a high impedance load for the first stage output. Capacitor C86 decreases the speed of the low-frequency section at high frequencies.

4.4.12 Output Protection and Attenuator

There are three output amplifier protection safeguards to protect this circuit against major damage under the severest accidental misuse, including accidental connection of line power to the FUNC OUT connector. These safeguards are:

1. An overvoltage sensing circuit that detects voltages that exceeds the ± 15V limits at the FUNC OUT connector. When an overvoltage is detected, the circuit opens all relays in the output attenuator circuits and disconnects the amplifier from FUNC OUT.
2. An in-line fuse to protect the amplifier in case the voltage is great enough to arc across the relay contacts. Should the fuse blow, a sensing circuit alerts the microprocessor.
3. Two voltage-limiting, high current diodes (CR57 and CR58) at the amplifier output that prevent an externally applied voltage from pulling the amplifier output line beyond the range of the ± 15V supplies.

4.4.12.1 Overvoltage Sense Circuit

The overvoltage sense circuit compares the voltage at FUNC OUT (through isolating 1 MΩ resistors R298 and R299) with the ± 15V power supplies at U20 pin 4 and U20 pin 6 respectively. If the voltage at FUNC OUT goes higher than + 15V or lower than − 15V, the appropriate comparator output (U20 pin 2 or U20 pin 1 respectively) goes negative. Since the outputs are wire-OR'd, when either output becomes negative it drives the comparator output at U20 pin 14 positive. This turns off Q38 and opens all relays to disconnect the amplifier from the output. The positive level at U20 pin 14 also signals the microprocessor (via the OAP line) that the output protection circuit has been activated. The microprocessor immediately signals the operator through the front panel display, the beeper and the GPIB. Removal of the external overvoltage immediately returns the output to its previous state and normal operation is resumed. The response of the relays is usually fast enough to prevent any damage whatsoever to the output amplifier with overvoltages up to 200 Vdc or 140 Vac.

4.4.12.2 Fuse Protection

Voltages greater than ± 200V may cause the relay contacts to arc and conduct. If such a condition occurs, a fast-acting fuse, F1 will generally blow soon enough to prevent, or at least minimize, damage to the instrument. A fuse sense circuit detects when the fuse is blown by pulling the output side of the fuse toward + 15V through a 1 MΩ resistor, R288. If the fuse is open during power-up or reset (K1 off), the sense point level rises higher (> + 13.6V) than the amplifier output would normally let it go, which switches output (U20-13) high. The microprocessor samples the logic level at the fuse-blown indicator line (FUB) and signals the operator through the front panel display and the GPIB bus.

4.4.12.3 Output Attenuator

All three output relays (K1, K2 and K3) are independently driven by Q39, Q40 and Q41 and controlled by logic lines OA0 and OA2 from the micro-

processor. OA0 determines whether or not the output amplifier is connected, while OA2 switches the attenuator in or out. K2 and K3 both operate from the OA2 line, and operate opposite of each other (when one is on, the other is always off).

There are five possible combinations of operating states for the three relays. They are:

1. Overvoltage circuit tripped (Q38 turned off).
2. OUTPUT OFF (0) mode.
3. OUTPUT ON (1) mode, no attenuation. Output voltages (amplitude + offset) programmed for greater than 1.00V.
4. OUTPUT ON (1) mode, 20 dB attenuation. Output voltages (amplitude + offset) programmed for 1.00V or less.
5. OUTPUT OFF, LO Z (2) mode. Output terminated in approximately 50 ohms.

Relay states for these five conditions are shown in simplified schematic diagram Figure 4-20. In this figure, R289-R292 and R295 are shown as a single 50Ω resistor; R293, R294, R296 and R297 are shown as a single 55.6Ω resistor.

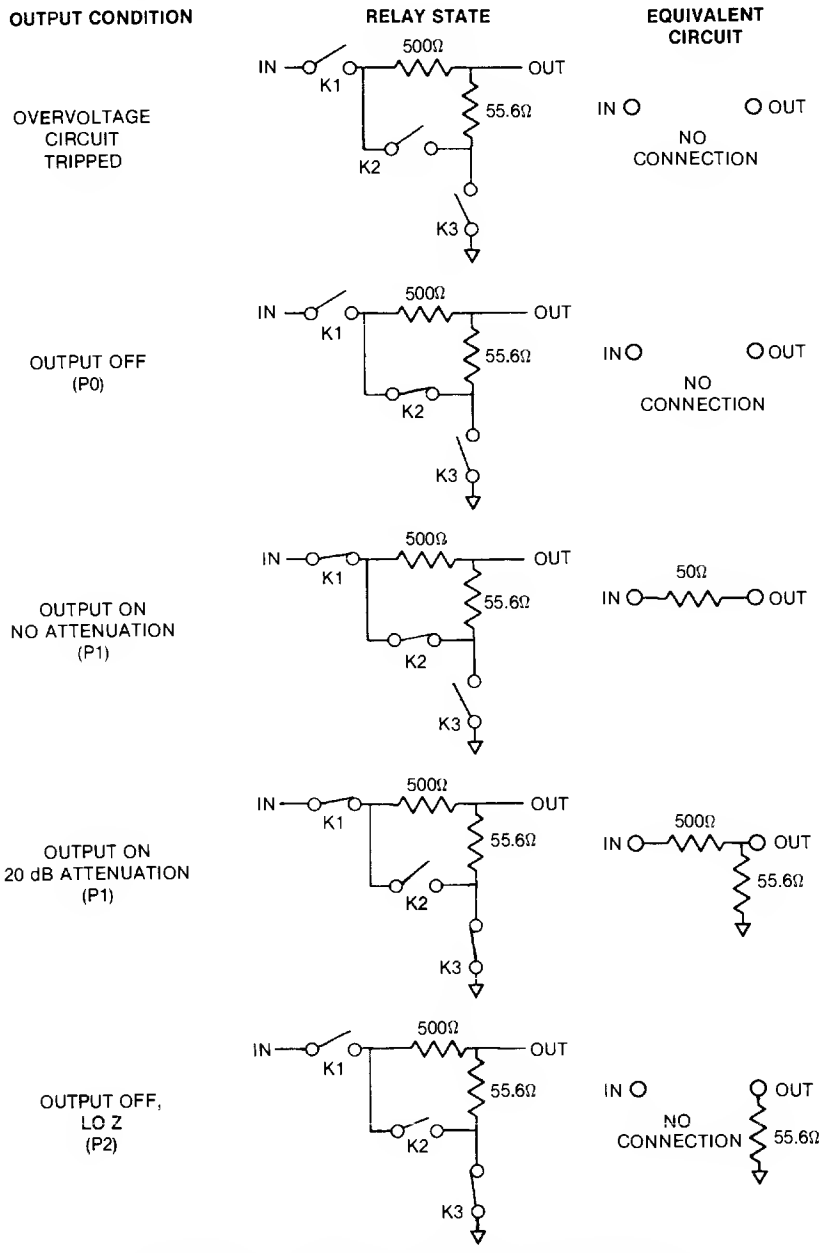


Figure 4-20. Output Attenuator Relay States

4.5 AUXILIARY BOARD CIRCUIT DESCRIPTION

The auxiliary board contains four major functional circuit groups. These are:

1. The synthesizer, which generates the reference frequency used by the main loop in the synthesized and external reference modes.
2. The main loop, which phase locks the function generator to an external reference within 5% of the programmed generator frequency, or to the output of the frequency synthesizer.
3. The burst counter, which holds the generator trigger line high for a predetermined number of output cycles.
4. The control logic circuits, which latch data from the data bus to provide data and control signals for the synthesizer and burst counter circuits.

During the following circuit description, refer to the Figure 4-2 block diagram and the schematic diagram of the synthesizer board, drawing number 0103-00-0978.

4.5.1 Control Logic

The control logic circuit consists of address decoder U1 and latches U2 through U7. Address decoder U1, when enabled by a logic low on the $\overline{ANA2}$ line, decodes the binary value on the ADR0 through ADR2 address lines and provides a momentary logic low on the corresponding clock line of one of the U2 through U7 registers. (For example, a binary address value of "000" selects U2, a value of "001" selects U3, etc.) When the register clock line returns to a logic high, it latches the data from the buffered data bus (J16 pins 1 through 8) onto the register output pins, where it is continuously available to the remainder of the circuits on the board. Each register is clocked by the microprocessor and address decoder at a time when the data on the buffered data bus is valid for that particular register.

4.5.2 Burst Counter

The burst counter holds the generator trigger line high for a predetermined number of output cycles when the burst mode is selected. The two circuit groups within the burst counter are the preset counter and the burst mode logic.

The preset counter is composed of NAND gates U8B and U8A, presettable 4-bit binary counters U9 through U13, and terminal count detector NAND gate U14. When the preset counter is enabled by the burst mode logic it preloads data from the control logic registers then counts square wave cycles from the generator, counting upwards from the preloaded value. When the final count value is reached, the circuit commands the burst mode logic to relinquish control of the generator trigger circuit.

Although U9 through U13 are capable of counting to 1,048,575 ($20^{20}-1$), the maximum count is limited to 1,048,200 by terminal count detector U14. This number corresponds to all 13 lines to the terminal count detector being at a logic high, and can be represented by the binary number $2^3 + 2^7 + 2^9 + \ldots + 2^{19}$. (Note that some of the counter outputs such as 2^0, 2^1, 2^2, 2^4, etc. are not used.) The binary number that will be loaded from the program registers into the preset counter is this maximum count minus the desired count plus one. (The burst mode logic will always allow one extra cycle after the preset counter reaches maximum count.)

The normal state of the preset counter is at its maximum count of 1,048,200. The output of terminal count detector U14 is at a logic low at maximum count, and this logic low inhibits NAND gate U8B, preventing the generator output square wave (SQS) from reaching the counter input. The logic high at the output of U8B enables NAND gate U8A to pass the first clock pulse from the burst mode logic to the counter.

The burst mode logic (U15A, U15B, U8C and U8D) is activated by a trigger pulse (TRGOB) from the synthesizer trigger logic, and returns the trigger pulse to the function generator board via the TRGI line (J16 pin 7). In the burst mode, the trigger pulse at TRGI is extended for the duration of the burst. When the burst mode is not selected, the output trigger pulse at TRGI is a copy of the input pulse at TRGOB.

In the burst mode, the BURST line is at a logic high, and the $\overline{BURST}$ line is at a logic low. The logic low on the $\overline{BURST}$ line disables NAND gate U8D and enables NAND gate U8C via the constant high at the U8D output. The logic low on the $\overline{BURST}$ line is also applied to the data input of flip-flop U15A.

Initially, the counter is in the maximum-count condition, and the output of the terminal count detector is at a logic low. This logic low is applied to the $\overline{LOAD}$ inputs of counter stages U9 through U13 to enable loading of the preset data at the next clock pulse. The same logic low disables NAND gate U8B to prevent the SQS square wave from clocking the counter, and enables NAND gate U8A (via the logic high on the U8B output) to allow the load pulse from U15A to clock the counter.

A positive logic transition at the TRGOB trigger input clocks the U15A Q output low. The negative-going

transition at the U15A Q output is inverted by U8A and applied to the counter clock inputs to load the preset data. As soon as the counter is loaded with preset data, it is no longer at the maximum count condition and the U14 output goes high, disabling the counter $\overline{\text{LOAD}}$ inputs and enabling NAND gate U8B. However, at this point, the SQS square wave input cannot yet reach the counter clock inputs because NAND gate U8A is disabled by a logic low from U15A.

After a time delay determined by R3 and C8, the logic low at the U15A Q output is applied to the U15B $\overline{\text{SET}}$ input to set the U15B $\overline{\text{Q}}$ output low. This low is inverted by U8C and provides a logic high on the trigger output line (TRGI) at J15 pin 7. The logic low at the U15B $\overline{\text{Q}}$ output is also applied back to the direct $\overline{\text{SET}}$ input of U15A to set the U15A Q output high. The logic high from the U15A Q output enables NAND gate U8A to pass square waves from the SQS input ot the counter.

When the counter reaches maximum count, the output of the terminal count detector U14 goes low, disabling NAND gate U8B and preventing SQS square waves from reaching the counter. U14 also supplies a logic low to the data input of flip-flop U15B. The next positive transition of the SQS square wave will clock the U15B $\overline{\text{Q}}$ output high, causing U8C to return the trigger output line TRGI to a logic low state.

When the burst mode is not selected, the BURST line is at a logic low state and the $\overline{\text{BURST}}$ line is at logic high. The logic low on the BURST line holds the $\overline{\text{CLEAR}}$ input of flip-flop U15B low, maintaining a logic high from the U15B $\overline{\text{Q}}$ output to enable NAND gate U8C. The logic high on the BURST line enables NAND gate U8D. Any trigger signal applied to the TRGOB line will be gated through U8D and U8C to the TRGI output.

4.5.3 Synthesizer Circuits

The synthesizer circuits generate the reference frequency used by the Main Loop in the synthesized or external reference modes. The major circuit groups within the synthesizer are the Synthesizer Reference, the Internal Synthesizer Loop, and the Synthesizer Frequency Dividers.

4.5.3.1 Synthesizer Reference

The Synthesizer Reference circuits include the 10 MHz reference oscillator, the reference shaper, the reference selector gates, and the divide-by-3125 frequency divider.

The 10 MHz reference oscillator used in the Wavetek 278 is a standard Pierce configuration with the combination of capacitor C12 and crystal Y1 resonant with capacitors C14, C15 and C16. This combination provides a 180° phase shift at 10 MHz when C14 is properly adjusted. Transistor Q2 provides an additional 180° phase shift to sustain oscillation. The output of the oscillator is approximately 1 Vp-p. The output goes to one of the two comparators in the U16 reference shaper, where it is converted to a TTL signal. This signal is then applied to the U17 TTL switch.

Transistor Q1 is used as a switch to turn the Pierce oscillator on or off. When the control line $\overline{\text{INTERNAL REF}}$ is low, transistor Q1 is turned off and the Pierce oscillator is allowed to run. When $\overline{\text{INTERNAL REF}}$ is high Q1 is biased on, allowing Q1 to conduct current through CR2. This lowers the voltage on the base of Q2, turning off the oscillator.

Reference shaper U16 is a dual comparator that converts the inputs from the 10 MHz reference oscillator and the P13 REF INPUT connector to TTL levels. The input from the reference oscillator (pin 12) is compared to ground potential (pin 11). The input from the P13 REF INPUT connector (via R11 and R12) is compared to a threshold voltage derived from the REF LEVEL SELECT line (via R15 and R14). The U16 comparator outputs (pins 9 and 4) are applied to reference selector gates U17. (The external reference from U16 pin 4 is also applied to the Main Loop circuits for use in the phase-lock mode.) When the REF LEVEL SELECT line is high, the threshold voltage (measured at the P13 REF INPUT connector) is 1.6V. When the line is low, the threshold voltage is 300 mV. R13 provides a slight amount of positive feedback to ensure rapid comparator switching and improved noise immunity. R11 and R12 ensure that the REF INPUT signal will be within the input range of the comparator. CR4 and CR5 prevent damage to the comparator from an excessive REF INPUT signal by preventing the externally applied signal from pulling the comparator input line above +5V or below ground potential.

NAND gates U17 select either the internal or the external 10 MHz reference from the U16 comparator output pins 9 or 4. A logic low on the $\overline{\text{INTERNAL REF}}$ line inhibits U17D. This logic low is inverted by U17A to enable U17B to pass the internal reference signal. When the $\overline{\text{INTERNAL REF}}$ line is high, it directly enables U17D and, via inverter U17A, disables U17B. U17C combines the reference signal from the enabled gate with a constant logic high from the disabled gate, and applies the 10 MHz TTL reference to the divide-by-3125 circuit and reference output selector gates U39.

The divide-by-3125 circuit is composed of integrated circuits U18 through U20. Each IC contains four independent frequency dividers (two each divide-by-2 and two each divide-by-5) that can be cascaded in any desired combination. U18 and U20 are both configured for divide-by-25 operation, and U19 for divide-by-5. The overall division ratio of 3125 divides the 10 MHz reference down to a frequency of 3200 Hz for use as a reference by the Internal Synthesizer Loop.

4.5.3.2 Internal Synthesizer Loop

The Internal Synthesizer Loop generates the 10 MHz to 24 MHz signal used as the input frequency to the Synthesizer Frequency Dividers. This signal (called VCO) is phase-locked to the 3200 Hz frequency generated by the Synthesizer Reference circuit, and can be varied over the 10 MHz to 24 MHz frequency range in 200 Hz increments.

The following circuit groups are part of the Internal Synthesizer Loop: The PLL frequency synthesizer, loop filter, level translator, voltage-controlled oscillator (VCO), and the variable modulus prescaler (VMP). Operation of the entire loop will be discussed after these individual circuits are described.

The U21 phase locked loop (PLL) chip contains the reference divider (÷ R), variable divider (÷ N), phase detector and lock detect circuit. (It also contains other circuits not used in the Wavetek 278.) The reference divider is hard-wired (by grounding pins 1, 2 and 18) for a division ratio of 16. The 3200 Hz reference frequency is divided by 16, and the resulting 200 Hz reference is applied to one input of the internal phase detector. The variable divider (÷ N) is programmed by serial data at the pin 11 data input. This data is clocked into a 16-bit internal shift register by low-to-high transitions on the pin 10 clock line. The first two bits control internal switches, which are not used in the Wavetek 278. The remaining 14 bits are a binary representation of the ÷ N division ratio, and are loaded most significant bit first. When the serial load is complete, a logic high on the pin 12 enable line latches the data in the shift register into the programmable ÷ N counter. The IC is capable of a ÷ N range of 3 to 16838, but the range used in the Wavetek 278 is from 4999 to 11999. The output of the ÷ N counter is applied to the other input of the internal phase detector, and is also at 200 Hz when the loop is locked.

The internal phase detector is a digital tri-state device. It produces negative-going pulses when the variable frequency is greater than the reference frequency or is leading it in phase. Positive-going pulses are produced when the variable frequency is less than the reference frequency or is lagging in phase. The output is in a high-impedance state when the two signals are of equal frequency and phase.

Pin 8 of U21 is the lock detector signal. It is normally used to indicate that the loop is unlocked, but in the Wavetek 278 it triggers the VMP circuit. A momentary low on the line indicates that a phase comparison has taken place.

Loop filter U23 converts the positive-going and negative-going pulses from the U21 phase detector to a steady dc frequency control voltage. The time constant of the filter is determined by C30 and the series value of R17 and R18. The time constant of the loop is therefore approximately 332 milliseconds. The damping of the loop is determined by R22. C29 is a high frequency bypass used to reduce noise in the filter. Voltage divide R19/R20 sets the voltage on U23 input pins 2 and 3 to 2.5 Vdc. The output of the loop filter U23-6 varies from approximately 11 Vdc to 3 Vdc.

Level translator U24 inverts the polarity of the U23 loop filter output and translates the voltage to the level required by the U25 voltage-controlled oscillator (VCO). The voltage at U24 input pins 2 and 3 is set to 4.3 Vdc by R25 and R26. Under normal operation the output at U24 pin 6 varies between 3 Vdc and 7 Vdc.

U25 is an emitter-coupled logic (ECL) voltage-controlled oscillator (VCO). The VCO is tuned by varying the voltage on varactor diode CR6. The frequency of the VCO is determined by the inductance of L1 and the capacitance of CR6. The ECL output levels at pin 3 are converted to TTL levels by Q3. The Q3 output frequency is divided by 2 by U26 to obtain a symmetrical square wave with fast rise and fall times. The 10 MHz to 24 MHz output of U26 (labelled VCO on the schematic) drives the Synthesizer Frequency Dividers and the VMP circuit.

U22 is a one-shot used to convert a negative-going transition at U21 PLL chip lock-detect output (pin 8) to a negative-going pulse of fixed duration. A logic low from U21-8 is applied to one input of NOR gate U22B, causing its output to go high. The same logic low is inverted by U22A, delayed by R21 and C46, and applied to the other input of U22B to cause its output to return low after a time delay determined by R21 and C46. The positive-going pulse at the U22B output is inverted by U22D and used to trigger the VMP circuit.

The variable modulus prescaler (VMP) circuit is a frequency divider that is capable of dividing either by 10 or by 11. Its purpose is to increase the "setability" of the Internal Synthesizer Loop. With a fixed divide-by-10 circuit, the VCO output could be varied in

2000 Hz increments. By using the ÷10/÷11 circuit, the VCO frequency can be changed in 200 Hz steps.

The VMP circuit consists of presettable 4-bit binary counters U28 and U29, type "D" flip-flops U27A and U27B, and NAND gates U30B and U30D. U28 divides the VCO output by either 10 or 11, depending on the number preloaded into it by U27A. U29 counts the number of divisions by 11. U27B latches the circuit into the divide-by-11 mode when it is strobed by the $\overline{\text{VMP SET}}$ pulse, and returns the circuit to the divide-by-10 mode when the required number of divide-by-11 cycles have been completed. U30B and U30D invert the positive-going "carry" pulses from counters U28 and U29.

Pins 3, 4, 5 and 6 are the preset data inputs for U28, and correspond to binary values "1", "2", "4" and "8" respectively. The "8" input (pin 6) is hard-wired to ground (logic "0") and the "4" input pin is hard-wired to +5V (logic "1"). The remaining two inputs are controlled by flip-flop U27A. When U27A is in the "set" condition (Q output high and $\overline{Q}$ output low) the total U28 preset value is a binary "5". When U27A is in the "clear" state, the total preset value is "6". U28 will count upwards from this preset value until it reaches the count of "15", at which time the "carry" output (pin 15) will go high. Therefore, the U28 division ratio is the maximum count (15) minus the preset value (either 5 or 6) plus one more clock pulse to reload the preset data. (In other words, the division ratio is equal to 16 minus the preload value.)

The U29 counter is similar to the U28 counter, except that it counts the number of divisions by 11. The preload data on the VMP0 through VMP3 lines is equal to 16 minus the desired number of divisions by 11. Note that this circuit cannot be set for zero or one division by 11, as this would require preloading the counter to 15 or 16. The counter cannot be set to 16, because it only counts from 0 to 15. The counter cannot be set to 15, because the constant logic high at the pin 15 "carry" output would be inverted by U30D and hold the U27B $\overline{\text{PRESET}}$ input low, preventing the $\overline{\text{VMP SET}}$ pulse from latching this circuit. (A method for circumventing this problem will be discussed shortly.)

The VMP circuit sequence of operation is as follows (assume the U29 preload information on lines VMP0 through VMP3 has a binary value of "14"):

1. Initially, U27A is in the "clear" state (Q output low, $\overline{Q}$ output high) enabling the $\overline{\text{LOAD}}$ input of U29 and causing the U28 preload inputs to have a binary value of "6".
2. A phase comparison in the U21 PLL chip causes the $\overline{\text{VMP SET}}$ line to be pulsed low. The low on the $\overline{\text{VMP SET}}$ line latches U27B in the "clear" condition ($\overline{Q}$ output high) placing a logic "1" at the data input of flip-flop U27A.
3. Counter U28 will complete its current divide-by-10 cycle. At the count of "15" the "carry" output (pin 15) will go high. This level will be inverted by U30B, placing a low at the U28 $\overline{\text{LOAD}}$ input.
4. The next positive transition of the VCO output will clock the preload value of "6" into U28, preparing it for another divide-by-10 cycle. The U28 inverted "carry" output at U30B will go high, clocking the VMP preload data (assumed to be "14" in this example) into U29. This same transition of the U28 inverted "carry" output will clock the logic "1" at the U27A data input through to the U27A outputs. With U27A in the "set" state (Q output high, $\overline{Q}$ output low) the low will be removed from the U29 $\overline{\text{LOAD}}$ input and the preload information for U28 will be changed to a binary "5". (However, this information will not be loaded into U28 until its $\overline{\text{LOAD}}$ input is again pullsed low by U30B and a clock pulse is received from the VCO output.)
5. U28 completes another divide-by-10 cycle (9 clock pulses to reach the count of "15", plus one more to load the preset data). At the end of the count cycle, the inverted "carry" output from U30B loads the preset value "5" into U28 and increments the U29 counter to "15". The high on the U29 "carry" output is inverted by U30D to latch U27B in the "set" condition ($\overline{Q}$ output low) removing the logic high from the U27A data input.
6. U28 completes a divide-by-11 cycle. The inverted "carry" pulse from U30B reloads U28 with a preset value of "5" and clocks U27A to the "clear" condition (Q output low and $\overline{Q}$ output high), enabling the $\overline{\text{LOAD}}$ input of U29 and changing the U28 preset data to "6".
7. U28 completes another divide-by-11 cycle. The inverted "carry" pulse from U30B loads U28 with a preset value of "6" and clocks U29 to reload the VMP preset data. With U29 no longer in the "15" state, the inverted "carry" puise from U30D returns high, releasing the U27B $\overline{\text{PRESET}}$ input, enabling it to accept the next $\overline{\text{VMP SET}}$ pulse.

During discussion of operation of the entire loop, refer to Figure 4-21, Simplified Block Diagram, Internal Synthesizer Loop, and Table 4-2, Examples of Internal Synthesizer Loop Division Ratios.

The 3200 Hz reference frequency from the Synthesizer Reference is divided by 16 by the ÷R frequency

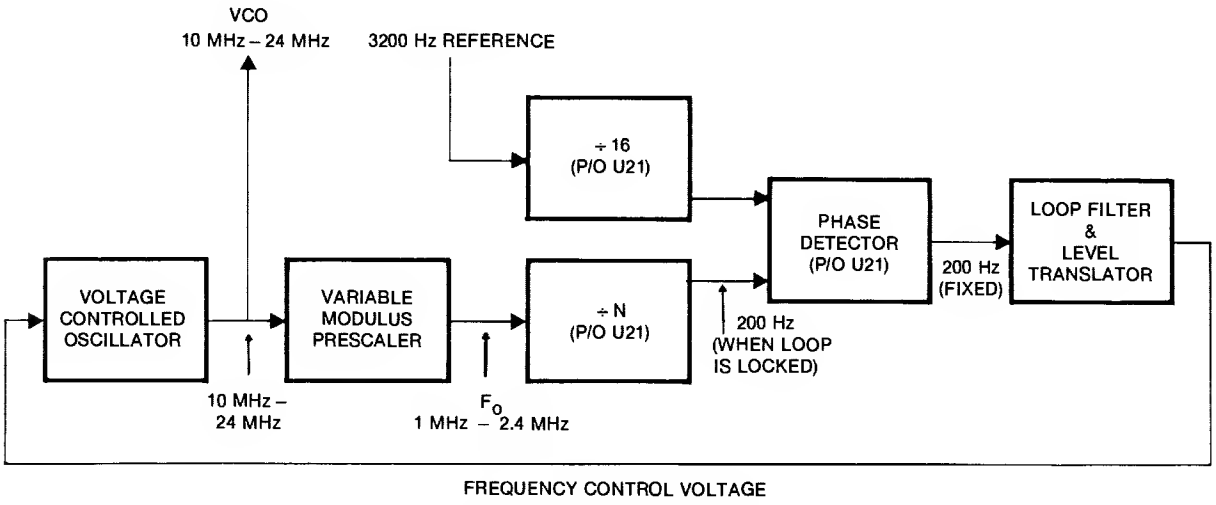


Figure 4-21. Simplified Block Diagram, Internal Synthesizer Loop

divider in U21, and the resulting 200 Hz frequency is applied to one input of the phase detector in U21. The output of the voltage controlled oscillator is divided by the variable modulus prescaler and the programmable (÷ N) divider circuit in U21, and applied to the other input of the U21 phase detector. The output of the U21 phase detector (via the loop filter and level translator) varies the frequency of the VCO until the output frequency of the programmable (÷ N) divider exactly equals the 200 Hz reference frequency.

Table 4-2 shows some examples of VCO output frequencies generated by various combinations of ÷ N division ratios and number of VMP ÷ 11 division cycles. Let's work backwards from the phase detector for the case of N = 5000 and the number of VMP ÷ 11 cycles = 2.

1. The reference frequency into the U21 phase detector is a fixed 200 Hz.
2. When the loop is locked, the two phase detector inputs will be equal in frequency; therefore the output of the ÷ N divider will also be 200 Hz.
3. If N = 5000, then 5000 cycles of input will be required for each cycle of output from the ÷ N circuit.
4. For 5000 cycles of input into the ÷ N circuit, the VMP circuit must provide 5000 cycles of output, and therefore must go through 5000 cycles of division.
5. If two of the VMP division cycles are division by 11, then the remaining 4998 cycles are division by 10.
6. For 5000 cycles of VMP output, the number of VMP input cycles is (2 × 11) + (4998 × 10) = 50,002.
7. If the VCO output is 50,002 cycles for each cycle of output from the ÷ N circuit, and the ÷ N output frequency is 200 Hz (cycles per second), then the VCO output frequency is 200 × 50,002 = 10,000,400 Hz.

It can be seen from the examples in Table 4-2 that incrementing the division ratio N will raise the VCO frequency by 2000 Hz, while incrementing the number of divisions by 11 in the VMP circuit will increase the VCO frequency by only 200 Hz.

Mathematically, the frequency equation for the loop is:

$$\frac{f_{vco}}{N*P+A} = \frac{f_{ref}}{R}$$

where

f_{vco} = the frequency of the voltage controlled oscillator

N = the PLL division ratio

P = the lower modulus of the variable modulus prescaler

A = the number of divisions by the upper modulus per phase compariosn

f_{ref} = the reference frequency

R = the reference division ratio

Table 4-2. Examples of Internal Synthesizer Loop Division Ratios

U21 Phase Detector Input Frequency Hz	U21 ÷ N Division Ratio	U21 Variable Divider Input Frequency		Number of VMP Frequency Divisions Per Phase Comparison			Number of VMP Input Cycles (VCO Output)	
		F_O Cycles Per Second (Hz)	Cycles Per Phase Comparison (F_O ÷ 200)	Total VMP Division Cycles	Number Of ÷ 11 Cycles	Number Of ÷ 10 Cycles	Cycles Per Phase Comparison	Cycles Per Second (Hz)
200	4,999	999,800	4,999	4,999	10	4,989	50,000	10,000,000
200	4,999	999,800	4,999	4,999	11	4,988	50,001	10,000,200
200	5,000	1,000,000	5,000	5,000	2	4,998	50,002	10,000,400
200	5,000	1,000,000	5,000	5,000	3	4,997	50,003	10,000,600
200	5,000	1,000,000	5,000	5,000	4	4,996	50,004	10,000,800
200	5,000	1,000,000	5,000	5,000	5	4,995	50,005	10,001,000
200	5,000	1,000,000	5,000	5,000	6	4,994	50,006	10,001,200
200	5,000	1,000,000	5,000	5,000	7	4,993	50,007	10,001,400
200	5,000	1,000,000	5,000	5,000	8	4,992	50,008	10,001,600
200	5,000	1,000,000	5,000	5,000	9	4,991	50,009	10,001,800
200	5,000	1,000,000	5,000	5,000	10	4,990	50,010	10,002,000
200	11,998	2,399,600	11,998	11,998	10	11,988	119,990	23,998,000
200	11,998	2,399,600	11,998	11,998	11	11,987	119,991	23,998,200
200	11,999	2,399,800	11,999	11,999	2	11,997	119,992	23,998,400
200	11,999	2,399,800	11,999	11,999	3	11,996	119,993	23,998,600
200	11,999	2,399,800	11,999	11,999	4	11,995	119,994	23,998,800
200	11,999	2,399,800	11,999	11,999	5	11,994	119,995	23,999,000
200	11,999	2,399,800	11,999	11,999	6	11,993	119,996	23,999,200
200	11,999	2,399,800	11,999	11,999	7	11,992	119,997	23,999,400
200	11,999	2,399,800	11,999	11,999	8	11,991	119,998	23,999,600
200	11,999	2,399,800	11,999	11,999	9	11,990	119,999	23,999,800
200	11,999	2,399,800	11,999	11,999	10	11,989	120,000	24,000,000

In this circuit P = 10,

and

$\frac{f_{ref}}{R} = \frac{3200}{16} = 200$. Therefore, the equation

reduces to:

$$\frac{f_{VCO}}{10N+A} = 200$$

This equation can be rearranged to the form:

$$f_{VCO} = 2000N + 200A$$

As previously mentioned, in this particular circuit A cannot be set to 0 or 1 because the U29 counter in the VMP circuit cannot be preset to 15 or 16. In these two cases, A is set to 10 or 11 and N is decremented by 1.

4.5.3.3 Synthesizer Frequency Dividers

The Synthesizer Frequency Dividers divide the 10 MHz to 24 MHz VCO frequency down to the range of 1 Hz to 9.9999 MHz. (For frequencies of 10 MHz and above, the VCO output is used directly, without frequency division.) The Synthesizer Frequency Dividers consist of binary divider U31, decade dividers U33 through U35, and 8-input multiplexers U32 and U36. Also included in this circuit group are the internal/external trigger selector gates and the reference output selector gates.

The 10 MHz to 24 MHz VCO frequency is applied to the clock input of 4-bit binary divider U31. U31 provides four simultaneous outputs with frequencies of VCO ÷ 2, VCO ÷ 4, VCO ÷ 8 and VCO ÷ 16. The four outputs of U31 are applied to U32, which selects one of them as the frequency source for the decade dividers. The microprocessor, via the BINARY A and BINARY B control lines, selects the binary divider output having the lowest frequency that is within the 1 MHz to 10 MHz input frequency range of the decade dividers. Table 4-3 shows the relationship between decade divider input frequency and binary divider division ratio.

U33 through U35 provide 6 decades of frequency division, down to frequencies as low as 1 Hz. These dividers all run constantly, and their outputs are all applied to 8-input multiplexer U36, along with the outputs of the VCO and the binary divider. U36 selects the input corresponding to the binary value on its three control lines from the microprocessor, and

applies the selected frequency to the selector gates for the main loop, buffered trigger output and reference output.

NAND gates U39 select either the synthesizer output or the 10 MHz reference from the Synthesizer Reference Circuit for application to the Reference Output amplifier. A logic high on the SYN/$\overline{\text{REF}}$ line enables U39A to pass the synthesizer output signal. The logic high is inverted by U39B to inhibit U39D, holding its output at a logic high. A logic low on the SYN/$\overline{\text{REF}}$ line inhibits U39A, and is inverted by U39B to enable the 10 MHz reference frequency to pass through U39D. U39C combines the outputs of U39D and U39A. The signal from the enabled gate is combined with a constant logic high from the disabled gate, and the selected signal is applied to the Reference Output amplifier.

U38 operates in a similar manner to select either the synthesizer output or the external trigger as the trigger source. A logic high on the INT/$\overline{\text{EXT}}$ TRIG line selects the synthesizer output; a logic low selects the TRGO signal from the trigger comparator on the function generator board. The selected source is applied to the burst counter circuit as buffered trigger output TRGOB.

Table 4-3. Binary Divider Frequency Ranges

Programmed Frequency Significant Digits	Decade Divider Input Frequency (MHz)	Binary Divider Division Ratio	VCO Frequency (MHz)
10000-12499	1.0000-1.2499	16	16.0000-19.9984
12500-24999	1.2500-2.4999	8	10.0000-19.9992
25000-49999	2.5000-4.9999	4	10.0000-19.9996
50000-99999	5.0000-9.9999	2	10.0000-19.9998

NOTE: For frequencies of 10 MHz and above, the VCO output is used directly, without binary or decade frequency division.

4.5.4 Main Loop Circuit

The main loop circuit allows the Wavetek 278 to be phase-locked to an external reference within 5% of the programmed generator frequency, or to the frequency synthesizer operated from an internal or external reference at a fixed frequency of 10 MHz. Figure 4-22, Generator Operation in Phase-Locked and Synthesized Modes shows the relationship between the function generator board and the synthesizer board in the phase-locked and synthesized modes.

The SQS square wave output of the function generator board is divided by two and applied to one of the inputs of the phase detector in the Main Loop circuit on the synthesizer board. (This phase detector should not be confused with the phase detector in the synthesizer circuits.) The other side of the phase detector is driven by either the synthesizer output or an external reference within 5% of the programmed generator frequency (also divided by two). The Main Loop phase detector and loop filter develop a dc voltage proportional to the phase or frequency difference of the two signals. This error voltage is summed with the frequency control voltage (VCO) from the function generator board, then returned to the function generator board as a modified frequency control voltage, VCGI. This VCGI voltage varies the function generator frequency until it is equal to the reference frequency at the other input of the Main Loop phase detector.

The P13 REF INPUT connector accepts a TTL or zero-crossing signal at the programmed generator frequency in the TTL LOCK and ZERO LOCK modes, or a TTL or zero-crossing signal at a fixed 10 MHz frequency in the TTL REFERENCE and ZERO REFERENCE modes. In the SYNTHESIZER mode, the internal 10 MHz crystal oscillator is used for reference.

Circuit groups within the Main Loop circuit are the synthesizer/phase lock selector gates, phase detector, charge pump, loop filter and summing amplifier.

NAND gates U37, controlled by the SYNTH/$\overline{\phi}$ SELECT control line, select either the output of the synthesizer or the output of the reference input comparator (U16). A logic high on the control line gates the synthesizer output through U37A; a logic low on the line is inverted by U37C to gate the ϕ LOCK IN signal through U37D. The selected output is applied through frequency divider U40A to the reference input of phase detector U41.

The square wave output of the function generator (SQS) is applied through frequency divider U40B to the variable frequency (V) input of U41. U40A and U40B divide the reference and variable frequencies by 2 to bring them within the maximum frequency limit of phase detector U41.

U41 is a digital phase detector that is driven by negative-going transitions of the reference frequency (R) and variable frequency (V) input signals. When the two input signals are in phase, both the U1 and D1 outputs remain high. When the R input (pin 1) leads the V input (pin 3) in phase, output D1 (pin 2) stays high and output U1 (pin 13) pulses low during the interval between negative transitions of the R and V signals. When V leads R, U1 stays high and D1 pulses low during this interval. These pulses are converted to

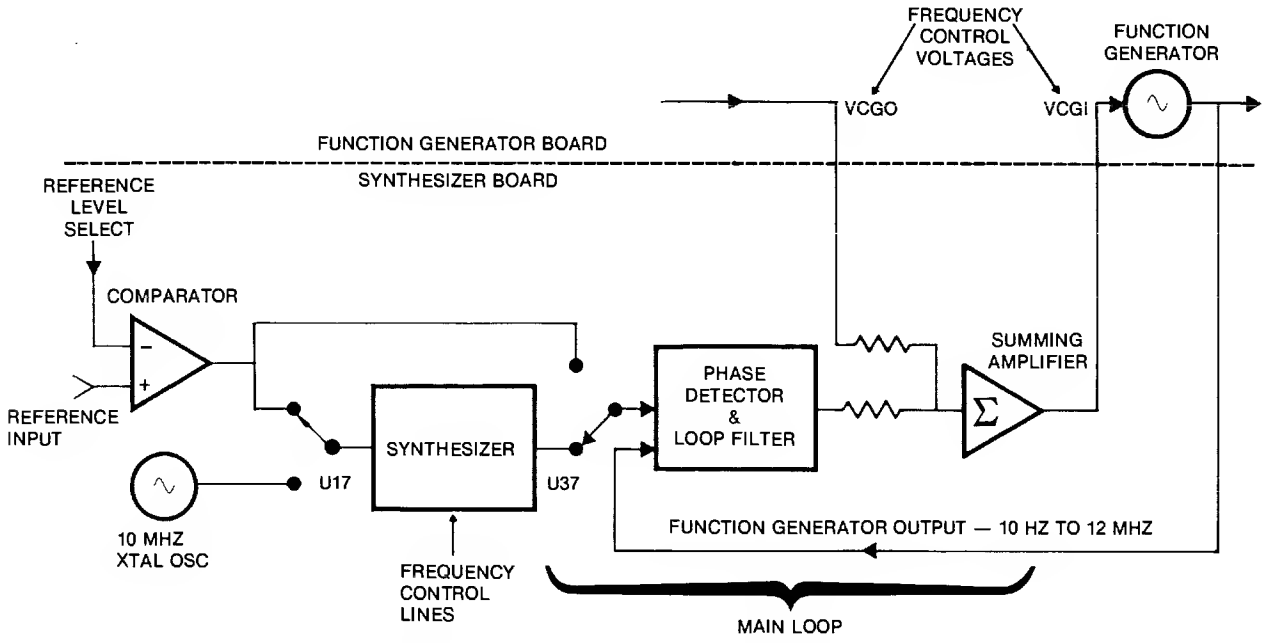


Figure 4-22. Generator Operation in Phase Locked and Synthesized Modes

a dc frequency control voltage by the charge pump and loop filter circuits.

The charge pump circuit consists of inverter U42, diodes CR8 through CR11, analog switch U43 and associated resistors. This circuit converts the U1 and D1 digital outputs of the phase detector to a single output that is either a positive current source, a negative current source, or is in a high-impedance (off) state. Figures 4-23 through 4-25 illustrate charge pump operation for the three possible combinations of logic levels on the U1 and D1 input lines. Voltages on these diagrams are simplified to illustrate theory of operation, and are not intended to represent **exact** circuit voltages. In these diagrams, logic levels are assumed to be exactly 0V and +5V, and the voltage drops across forward-biased diodes are neglected.

Figure 4-23 shows circuit operation when inputs U1 and D1 are both high. The logic high at the U1 input is inverted by U42, and holds the junction of CR8 and CR9 at zero volts. The logic high at the D1 input holds the junction of CR11 and CR10 at +5V. The +2.5V level from the loop filter input is fed back through R51 to the junction of CR9 and CR10, reverse biasing both diodes to maintain the circuit in the "off" condition.

Charge pump operation with the U1 input low and the D1 input high is shown in Figure 4-24. The logic low at the U1 input is inverted by U42 to bias the cathode of CR8 to +5V. The logic high at the D1 input is applied through CR11 to bias the cathode of CR10 to +5V. Current flows from the +15V supply, through R45-R47, CR9 and R51 into the loop filter. The values of R45-R47 are chosen to be much larger than the value of R51, so that the voltage at the midpoint of the R51/R45-R47 voltage divider does not exceed +5V. With this midpoint limited to +5V or less, CR8 and CR10 are both reverse biased, and the only current path into or out of the loop filter is through R45-R47, CR9 and R51.

Circuit operation with the D1 input low and the U1 input high is shown in Figure 4-25. The logic high at the U1 input is inverted by U42, and applied through CR8 to the junction of CR8 and CR9. The logic low at the D1 input biases the CR11 anode to 0V. Current flows from the loop filter, through R51, CR10 and R48-R50 to the −15V supply. The values of R48-R50 are chosen to be much larger than the value of R51, so that the voltage at the midpoint of the voltage divider formed by R51 and R48-R50 does not drop to less than zero volts. With this midpoint limited to zero volts or more, CR9 and CR11 are both reverse biased, and the only current path into or out of the loop filter is through R51, CR10 and R48-R50.

Solid-state analog switches U43A and U43B are opened by a logic high on the 10-99.9 Hz line when the generator is programmed to this frequency range. Opening the switches removes R46 and R49 from the circuit, reducing the current into and out of the loop

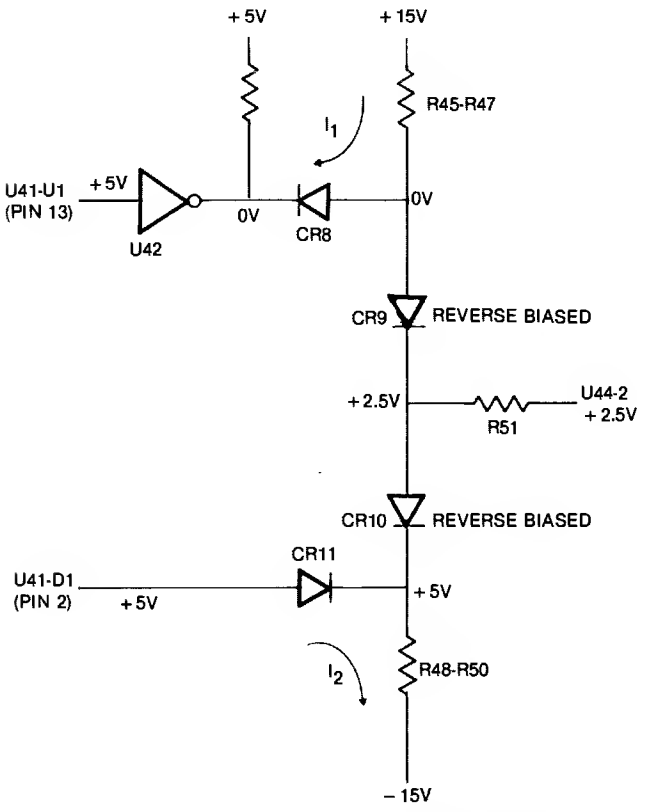


Figure 4-23. Charge Pump Operation With Both Inputs High

filter. This has the same effect as increasing the value of R51, which would lower the frequency of the loop filter.

Loop filter U44 integrates the positive-going and negative-going pulses from the charge pump circuit to provide a dc frequency control voltage for phase-locking the function generator. The filter is similar to the one in the internal synthesizer loop, with the exception that the filter is band-switched by solid-state switches U45A through U45D. For the 1K-99.9K range, the time constant of the filter is determined by R51 and C67. Loop damping is controlled by R41. C66 is a high frequency bypass used to reduce noise in the filter. Other filter ranges are identical except for component values. Filter range is selected by a logic low on one of the U45 control lines.

R52 and R53 set the voltage at the non-inverting input (pin 3) of U44 at +2.5V. During normal operation (when the Main Loop is locked) operational amplifier U44 will drive its output to whatever voltage is required to maintain a zero voltage difference between its two inputs; therefore this +2.5V level is also present at inverting input pin 2. However, there is no dc feedback path in the loop filter, and the operational amplifier output cannot exceed the ±15V value of the supply voltages. Therefore, when the loop is unlocked, the voltage at the pin 2 inverting input can vary from this +2.5V value. This deviation is detected by the Lock Detect circuit, which signals the microprocessor via the LOCK DET line.

Summing amplifier U48 combines the output of the loop filter with the VCGO frequency control voltage from the function generator board, and returns the modified frequency control voltage to the function generator board as VCGI. In the phase-lock and synthesized modes, a logic low on the $\overline{VCG}$ line closes series switch U47D and, via inverter U47A, opens shunt switch U47C to apply the loop filter output to the summing amplifier. In other modes, the switches disconnect the loop filter from the summing amplifier and the VCGI voltage is equal to the VCGO voltage. R59 adjusts the offset of summing amplifier U48.

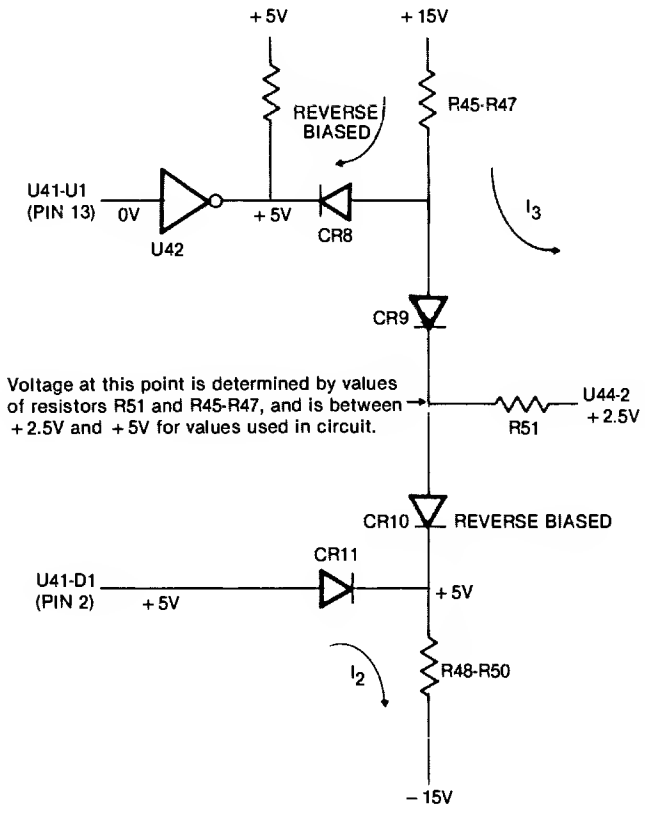


Figure 4-24. Charge Pump Operation With U1 Input Low

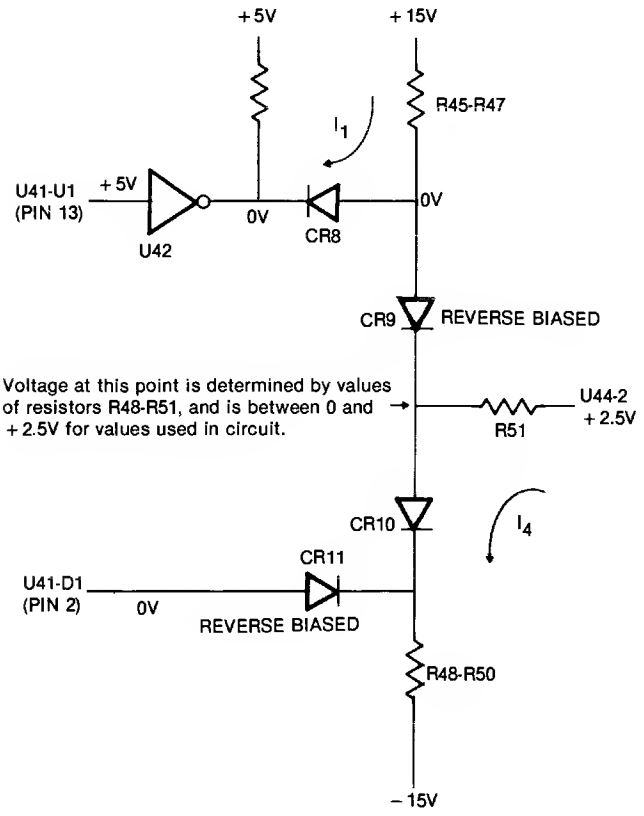


Figure 4-25. Charge Pump Operation With D1 Input Low

4.5.5 Lock Detect Circuit

The Lock Detect circuit consists of two comparators with their outputs both connected to a common pull-up resistor. The threshold of the U46A non-inverting input (pin 3) is set to 2.7 volts by R62 and R63. R65 and R66 set the threshold at the inverting input (pin 6) of U46B at 1.0V. The voltage from the loop filter inverting input is applied to the inverting input (pin 2) of U46A and to the non-inverting input (pin 5) of U46B. A voltage greater than 2.7V will cause U46A to pull the LOCK DET line low; a voltage less than 1.0V will cause U46B to pull the LOCK DET line low. The microprocessor response to the LOCK DET line going low is digitally filtered (delayed) to ignore normal switching transitions on this line. Typical response time is 4 seconds. When the loop is locked, this line is high.

Note that the lock detect circuit detects unlock of only the **main** loop and **not** the **internal synthesizer** loop. Removal of the 10 MHz external reference from the front panel REF IN connector in modes 5 or 6 will cause the internal synthesizer loop to go out of lock; in most cases the main loop will remain locked to the output of the unlocked synthesizer.

4.5.6 Reference Output Amplifier

The Reference Output amplifier is almost identical to the Sync Driver discussed in section 4.4.6 of the manual. Push-pull emitter followers Q4 and Q5 are biased on by the voltage drops across diodes CR12 and CR13. Emitter resistors R75-R78 provide negative feedback to prevent thermal runaway. Collector resistors R71-R74 and R83-R84 protect the transistors from overvoltage at the output connector. Collector bypass capacitors C80 and C82 prevent large signal swings at high frequencies that would reduce the gain of the transistors. High-frequency response is also improved by C79 and C81, which bypass base resistors R70 and R80.

4.5.7 Power Circuits

The ±15V lines and the +5V line enter the board at J17, and are filtered by ferrite beads FB1 through FB3 and C9-C11. Separate ±15V lines, labelled +15V-1 and −15V-1 on the schematic, are provided for the Reference Output circuit. A separate, isolated +5V supply for the U21 PLL and U25 VCO circuits (labelled +5VISO on the schematic) is derived from the +15V supply by three-terminal regulator VR2. The negative supply (−5VISO) for the U16 trigger comparator is generated from the −15V supply by regulator VR1.

4.6 MODEL DIFFERENCES

Wavetek Model 278 Function Generators with serial numbers less than 7230039 have several minor differences in the Microprocessor/Power Supply Board. Section 7 contains a schematic diagram (drawing number 0103-00-0919) of the earlier board revision. On the earlier version of the Model 278 Microprocessor/Power Supply Board:

1. $\overline{\text{MASTER RESET}}$ capacitor C1 was 100 μF, 16V. The $\overline{\text{MASTER RESET}}$ function ($\overline{\text{MR}}$) was performed entirely by charging this capacitor through R8; operational amplifier U27 was not used in the $\overline{\text{MASTER RESET}}$ circuit.
2. Operational amplifier U27A was used in the battery test circuit as a voltage follower amplifier providing an output equal to the comparator reference voltage. It was used to convert the ±15V output of the U27B comparator to TTL logic levels by summing the two voltages through R30 and R31.
3. The second RAM (U12) and memory backup battery BT1 were optional (Option 001).

4. There was no RAM PWR connection to auxiliary connector J4-19.
5. Alternate bus driver U8A pin 11, the DIRECTION CONTROL line (DC), was connected to +5V.
6. IEEE 488 Bus Driver U8B pin 1, the SEND/$\overline{\text{RECEIVE}}$ line (S/$\overline{\text{R}}$), was connected to +5V.
7. The $\overline{\text{CHIP ENABLE}}$ ($\overline{\text{CE}}$) input of U9 (pin 20) was connected to the ROM1 line.
8. The $\overline{\text{CHIP ENABLE}}$ ($\overline{\text{CE}}$) input of U10 (pin 20) was connected to the ROM2 line.
9. The $\overline{\text{ANA2}}$ and $\overline{\text{ANA3}}$ lines were buffered by auxiliary buffer U28 (pins 4,6,16 and 14) and appeared at the auxiliary connector J4 (pins 12 and 13) as $\overline{\text{BANA2}}$ and $\overline{\text{BANA3}}$.
10. Ground test points TP3, TP4 and TP5 were not present on the earlier revision board.
11. If applied power is interrupted and immediately reapplied, the instrument circuits may "hang up". A 3 second wait before reapplying power ensures normal instrument operation.

SECTION 5
CALIBRATION

5.1 FACTORY REPAIR

Wavetek maintains a Customer Service department. If an instrument is returned to Wavetek for repair or calibration, a detailed description of the specific problem should be attached to minimize turn around time.

5.2 CALIBRATION

> *NOTE*
>
> *The completion of the calibration procedure returns the instrument to correct alignment.* ***CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS.*** *Instrument specifications are given in Section 1 of this manual.*

Table 5-1 lists the equipment required to perform the calibration procedures in table 5-2.

The setup for each calibration step and a displayed operator cue are contained within the firmware. Calibration steps and cues can be accessed by pressing RCL 1001 EXEC, RCL 1002 EXEC, etc. for each step of the calibration procedure in table 5-2. Calibration points are shown in figures 5-1 through 5-3.

Periodic calibration is needed because of component aging, which depends on instrument on-time and environment. Use six months as an initial calibration period.

If possible keep records of the parameter values and modify the time between calibration if the records indicate.

To gain access to the Microprocessor/Power Supply board (steps 1 to 3), remove the bottom cover (2 screws).

To gain access to the Function Generator (steps 4 to 28) and Synthesizer boards (steps 29 and 30), remove the top cover (2 screws), next remove the two screws on the right of the Synthesizer board, and lift the Synthesizer board up to access Function Generator board adjustments(the Synthesizer board pivots on the left side).

NOTE

1. *EXEC (Execute), required to implement parameter value change, has been omitted from the calibration procedure.*
2. *Each step (RCL 1001, 1002 etc) also can be incremented and executed by using the cursor control (ref: paragraph 3.6).*
3. *When using the Function Output BNC, it must be terminatzed with a 50Ω termination.*

Table 5-1. Calibration Test Equipment

Instrument	Suggested Model	Comment
Digital Voltmeter	Fluke 8050A	DC accuracy: 0.01% AC Accuracy (true rms): 0.2%
Distortion Analyzer		Frequency range: 5 Hz to 100 kHz Distortion measurement: 0.1 to 100%
Frequency Counter		Frequency range: 0.5 Hz to 13 MHz Frequency accuracy: ±1 ppm
Oscilloscope		
Main frame	Tektronix 7904	Bandwidth: dc to 500 MHz
Plug-in		
Vertical Amplifier	Tektronix 7A26	Bandwidth: dc to 200 MHz Sensitivity: 5 mV to 5V/div Input impedance: 1 MΩ
Dual Time Base	Tektronix 7B53A	Time/div: 5 ns to 5 s
Sampler	Tektronix 7S14	Bandwidth: dc to 1 GHz

Table 5-1. Calibration Test Equipment

Instrument	Suggested Model	Comment
Terminations	Tektronix 011-0129-00 Tektronix 011-0049-01	50Ω ± 0.1%, 2W 50Ω ± 2.0%, 2W
Attenuator	Tektronix 011-0059-02	10X, 50Ω, 2W
Coax Cable	Tektronix 012-0057-01	50Ω, 3 ft length

Amplitude and Offset calibration requires a 50 ± 0.05Ω termination. If a precision termination is not available, a correction factor (K) can be derived, which can be used to calculate a normalized calibration value.

K is derived as follows:

$$K = \frac{R + 50}{2R}$$, where R is the value of the terminator used.

To calulate a normalized calibration value, divide the value from Desired Results by K. Or, multiply the measurement by K, which should equal the value from desired results.

Table 5-2. Calibration Procedure

NOTE: Open column indicates previous entry remains applicable

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
	NOTE: Steps 1 through 3 are power supply adjustments (see figure 5-1).						
1	+15V SUPP, R39	DVM (dc mode)	J3-1, TP2 (GND)	RCL 1001	R39	+15 ± .002 Vdc	
2	−15V SUPP, R47		J3-5, TP2 (GND)	RCL 1002	R47	−15 ± .002 Vdc	
3	−10.24V REF, R16		TP1, TP2 (GND)	RCL 1003	R16	−10.24 ± .002 Vdc	
	NOTE: Steps 4 through 28 are function generator adjustments (see figure 5-2)						
4	NODE BAL, R99	DVM (dc mode)	J23-9, TP1 (GND)	RCL 1004	R99	0 ± 1.0 Vdc	Move VCG jumper to E9 and E10 (Ref: figure 5-2).
5	TRI BALANCE, R60		J23-7, TP1 (GND)	RCL 1005	R60	0 ± .002 Vdc	
6	VCG ZERO, R11		VCG IN BNC (Front Panel)	RCL 1006	R11	0 ± .001 Vdc	
7	HI SYMM, R23	Oscilloscope	FUNC OUT (terminate with 50Ω)	RCL 1007	R23	50% Duty Cycle ±0.5 μs	
8	LO SYMM, R15			RCL 1008	R15	50% Duty Cycle ±0.5 μs	
9	LO FREQ, R12	Frequency Counter	FUNC OUT (terminate with 50Ω)	RCL 1009	R12	10 ± .1 Hz	
10	HI FREQ, R8			RCL 1010	R8	999 ±1.0 Hz	Steps 9 and 10 interact; repeat if necessary.
11	1 MHz, C43			RCL 1011	C43	1 ± .001 MHz	After making the initial adjustments in steps 11 and 12, record the frequency in each step. Place the synthesizer board in the operating position. Record the new frequency for each step. Note the difference in frequency. Lift up the synthesizer board. Increase the frequency by the frequency difference. Repeat steps 11 and 12 if necessary.
12	9.99 MHz, R45			RCL 1012	R45	9.99 ± .01 MHz	

Table 5-2. Calibration Procedure (Continued)

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
13	100 kHz, C45	Frequency Counter	FUNC OUT (terminate with 50Ω)	RCL 1013	C45	100 ± .1 kHz	
14	999 kHz, R46			RCL 1014	R46	999 ± 1 kHz	Steps 13 and 14 interact; repeat if necessary.
15	10 Hz SYM, R117	Oscilloscope		RCL 1015	R117	Symmetry 50% ± .1%	
16	0.999 Hz, R105	Frequency Counter		RCL 1016	R105	.999 ± .001 Hz	
17	99.9 Hz, R112			RCL 1017	R112	99.9 ± .1 Hz	
18	SINE DIST	Distortion Analyzer	FUNC OUT (terminate with 50Ω)	RCL 1018	R142 R154 R157 R255	<.3%	Adjust for minimum distortion.
19	MULT BAL, R241	Oscilloscope		RCL 1019	R241	≤.070 Vp-p	Adjust for minimum amplitude variation. Steps 18 and 19 interact; repeat if necessary.
20	OFFSET 0, R237	DVM (dc mode)	FUNC OUT (terminate with .1% 50Ω load)	RCL 1020	R237	0 ± .005 Vdc	
21	OFFSET +5, R208			RCL 1021	R208	5 ± .005 Vdc	
22	HI AMPL, R242	DVM (ac mode)		RCL 1022	R242	3.536 ± .01 Vac	
23	LO AMPL, R251			RCL 1023	R251	.357 ± .002 Vac	
24	TRI AMPL, R148	DVM (ac mode)		RCL 1024	R148	2.887 ± .003 Vac	
25	SQR LOWER, R168	DVM (dc mode)		RCL 1025	R168	−5 ± .005 Vdc	
26	SQR UPPER, R164			RCL 1026	R164	5 ± .005 Vdc	
27	ATTEN ADJ, R295			RCL 1027	R295	.500 ± .001 Vdc	
28	WAVEFORM C97, C122, R96	Oscilloscope with Sampler Plug in	FUNC OUT (terminate with X10, 50Ω attenuator)	RCL 1028	C97 C122 R96	Aberrations ≤3.3% ± 40 mV Rise/Fall <14.5 ns	Move VCG jumper to E10 and E11.
	NOTE: Steps 29 and 30 are synthesizer adjustments (See figure 5-3).						
29	AUX VCG ZERO	DVM (dc mode)	Measure differentially between TP1 and TP2 on the synthesizer board.	RCL 1029	R59	0 ± .0002 Vdc	
30	10 MHz REF ADJ	Counter	REF OUT (TTL Level)	RCL 1030	C14	10 ± .000020 MHz	

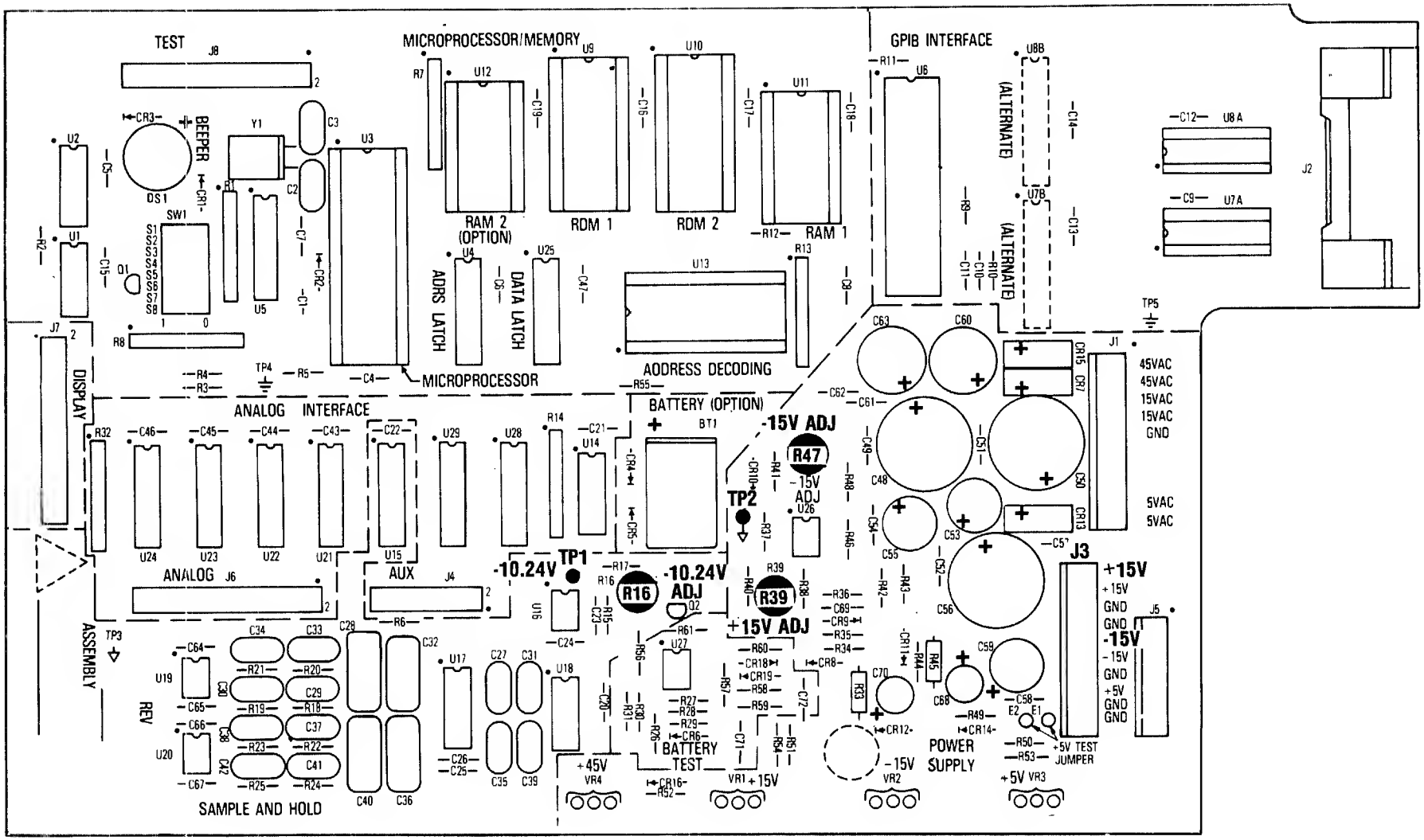


Figure 5-1. Microprocessor/Power Supply Calibration Point Locations

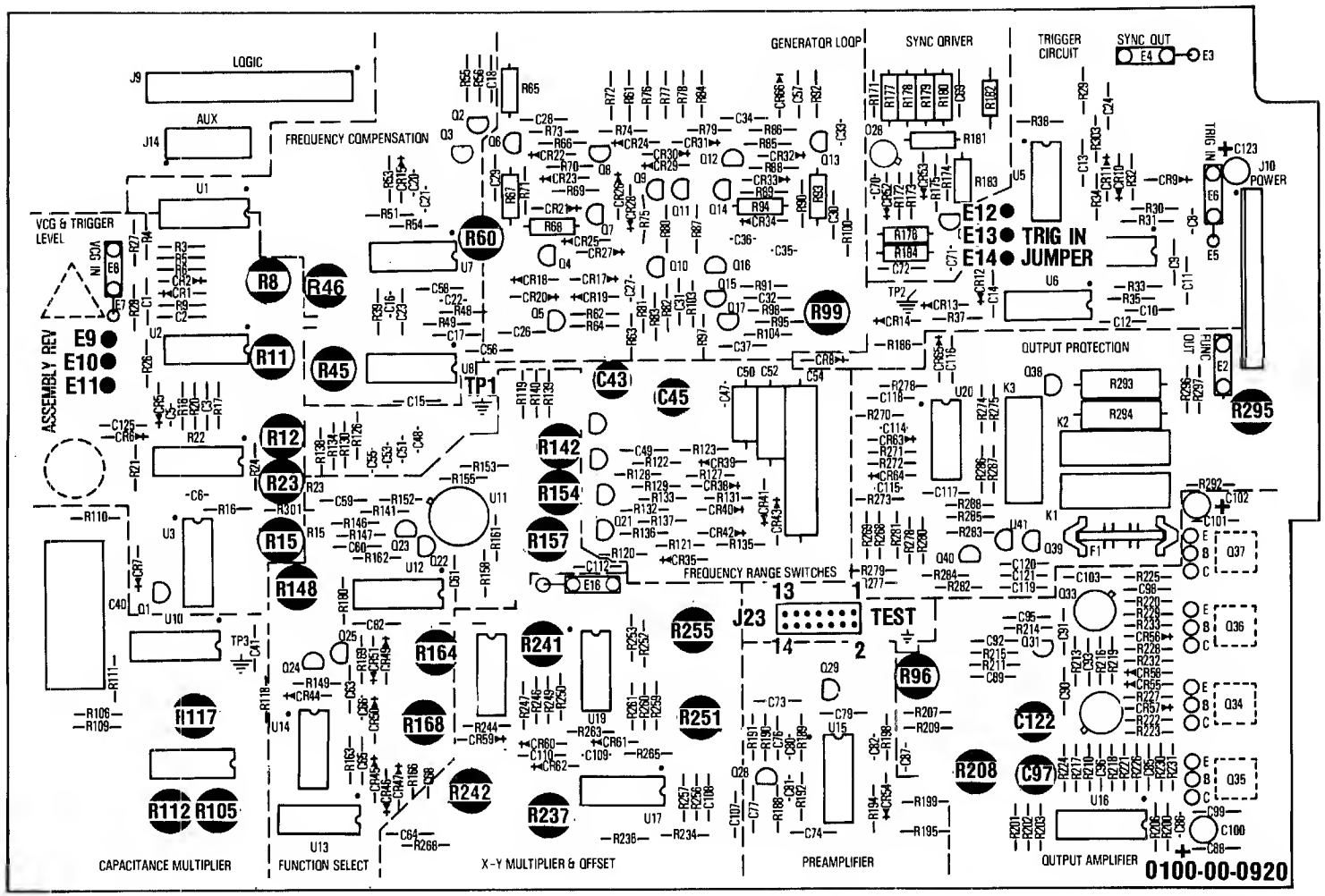


Figure 5-2. Function Generator Calibration Point Location

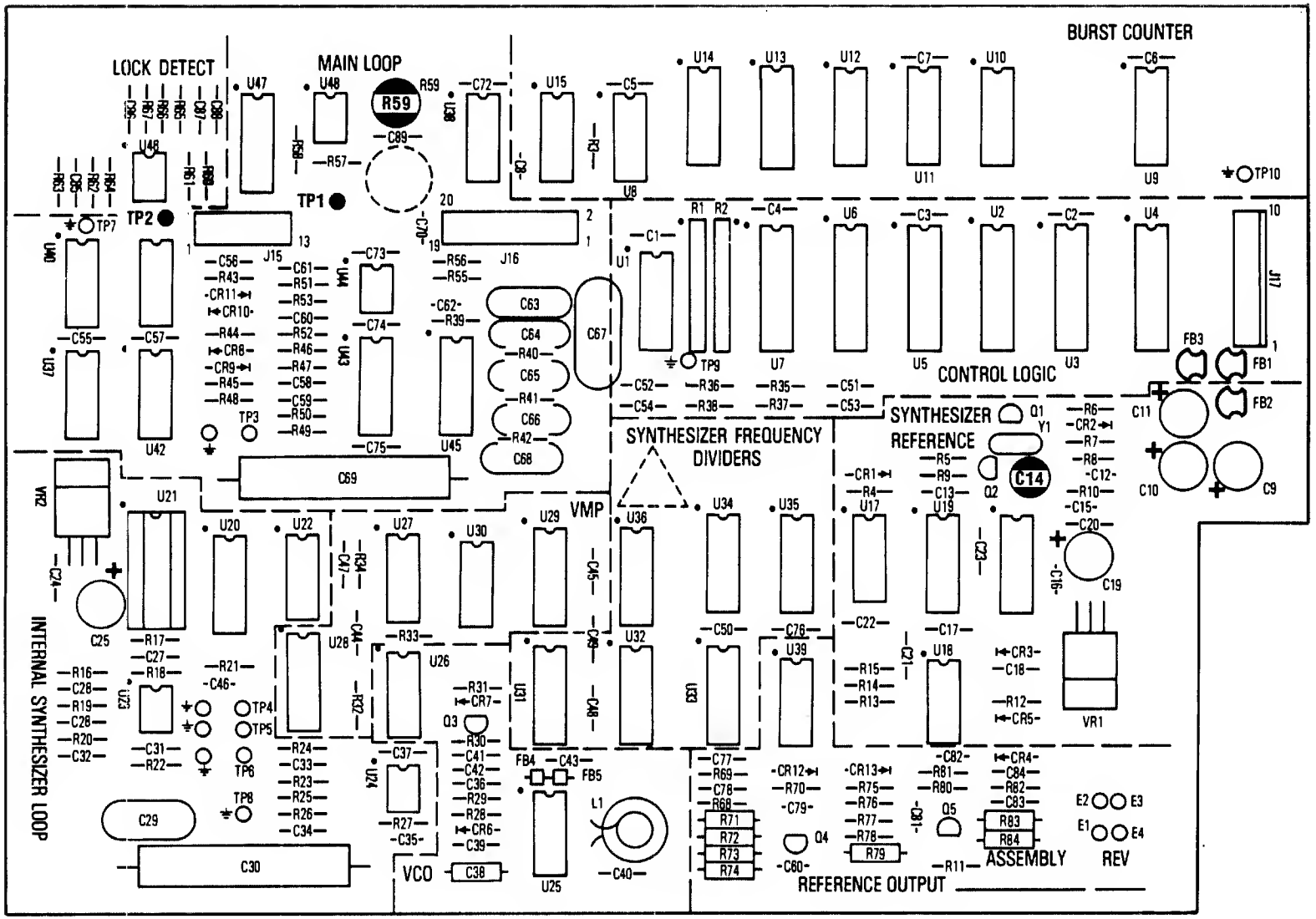


Figure 5-3. Synthesizer Board Calibration Point Locations

SECTION 6
TROUBLESHOOTING

6.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 BEFORE YOU START

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which, if applied consistantly, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the functional description and the detailed circuit description in conjunction with the schematic. Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as the block relationships.

6.3 TROUBLESHOOTING

Table 6-1 gives an index of common symptoms. For each symptom a troubleshooting step is referenced that will aid in the solution of the problem. Individual component troubleshooting is given in paragraph 6.4 recommended test equipment is given in paragraph 5.2 and circuit schematics are in the back of this manual.

In all problems:

1. Double check for proper parameter settings.
2. Verify power supplies are in specification.
3. Calibrate or rule out calibration as a problem.
4. Inspect components, wiring and circuit boards for heat damage.
5. Recalibrate as necessary after circuit repair.

Find the instrument symptom in table 6-1 and proceed as directed to the proper troubleshooting step. After verifying the referenced step is okay, proceed to the following step unless directed otherwise.

Table 6-3 provides voltages and waveforms for circuits on the Function Generator Board. These measurements were made with the default instrument parameters automatically selected at power-on or after pressing the RESET key, except that the output is turned on (OUT 1).

Tables 6-4 through 6-8 are truth tables of the logic states for the lines controlling frequency ranges, output relays, waveform functions, trigger modes and trigger slope.

Table 6-1. Symptoms

Symptom	Table 6-2 Step
Display does not light	1.1-1.3
Display is not "WAVETEK 278" at power up	2
"BATTERY LOW" displayed	3
Keyboard has no effect	4
Cannot recall stored settings	5
Won't work on GPIB	6
Keyboard will not work with unit on GPIB	7
No output or incorrect output at FUNC OUT (output on)	8
No output or incorrect frequency	8.1
High frequency incorrect, sine distortion excessive at low frequencies, or no output	8.2
Sine distortion excessive, no output, or no sync output	8.3
No output or frequency incorrect below 100 Hz	8.4
Excessive sine distortion, amplitude errors, or no output	8.5
Offset errors or no output	8.6
Output offset or no output	8.7

Table 6-1. Symptoms (Continued)

No triangle out	9
No square out	10
Trigger or gated mode error	11
No burst or incorrect burst count	12
Internal trigger does not function or is inaccurate	13
Synthesized frequency inaccurate in mode (4)	14
Will not lock to an external reference	15
"LOOP NOT LOCKED" displayed	16
No reference output	17
5th frequency digit will not change in mode 4	18

6.4 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.4.1 Transistor

1. A transistor is defective if more than one volt is measured across its base-emitter junction in the forward direction.
2. A transistor when used as a switch may have a few volts reverse bias voltage across base emitter junction.
3. If the collector and emitter voltages are the same, but the base emitter voltage is less than 500mV forward voltage (or reversed bias), the transitor is defective.
4. A transistor, when used as a linear amplifier, is defective if its base current is larger than 10% of its emitter current (calculate currents from voltage across the base and emitter series resistors).
5. In a transistor differential pair (common emitter stages), either their base voltages are the same in normal operating condition, or the one with less forward voltage across its base emitter junction should be off (no collector current); otherwise, one of the transistors is defective.

6.4.2 Diode

A diode (except a zener) is defective if there is greater than one volt (typically 0.7 volt) forward voltage across it.

6.4.3 Operational Amplifier

1. The "+" and "−" inputs of an operational amplifier will generally have less than 15 mV voltage difference when operating under normal conditions except when used as a comparator.
2. When the output of the amplifier is connected to the "−" input (voltage follower connection), the output should be the same voltage as the "+" input voltage; otherwise, the operational amplifier is defective.
3. If the output voltage stays at maximum positive, the "+" input voltage should be more positive than "−" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.4.4 FET Transistor

1. No gate current should be drawn by the gate of a FET transistor. If so, the transistor is defective.
2. The gate-to-source voltage for a junction FET (JFET) is always reverse biased under a normal operating condition; e.g., the source voltage is more positive than the gate voltage for a N-Channel JFET such as 2N5485, and the source voltage is more negative than gate voltage for a P-Channel JFET such as 2N5462. Otherwise, the FET is defective.

6.4.5 Capacitor

1. Shorted capacitors have zero volts across their terminals.
2. Opened capacitor can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.

6.4.6 Digital TTL IC's (e.g. 7400 Series)

1. The device is operating correctly if the output high state is $> +2.4V$ and low state is $< +0.5V$.
2. The input must show the same two levels as in step 1. If the levels are between $+0.8V$ and $+2.0V$, the connection to the driving circuit output is open.

Table 6-2. Troubleshooting

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
1.1	Display does not Light	AC Power a. Power Source b. Power Cord c. Power Fuse d. Power Selection e. Power Switch	— — — — — —	— — — — — —	— — — Rear panel Rear panel Inside rear panel	
1.2		DC Power a. +45V supply b. +5V supply c. ±15V supply	 4.2.6.2 4.2.6.1 4.2.6.3	 VR4, CR15-16, C60,63 VR3, CR13-14, C56,59 VR1-2, CR7-12, U26, C48,50,53,55	 1094/3/A4-7 1094/3/B4-7 1094/3/D3-7	
1.3		Display a. Supply Voltages b. Filament Driver c. Segment and Digit Drivers d. Fluorescent Display	 4.3.1	 J11 U8, CR3-4, C14-15 U1-5, CR1-2 V1	 0921/1/C7 0921/1/C3 0921/1/C4-7 0921/1/C1-2	
2	Does not display "WAVETEK 278" at power-up	Microprocessor section a. Reset Circuit b. E-clock c. Address Strobe (AS) d. Address/Data Bus (AD) e. Address Bus (ADR) f. Microprocessor Software	 4.2.3 4.2.1.1 4.2.1.1 4.2.1.1 4.2.1.2 4.2.7	 U3,27, CR1-2, 18-19 U3, 6, 13, 25 U3, 4 U3,4-6,9-12 U3-4,6,9-15,28 U9-10	 1094/1/C7, 2/A3 1094/1/D6 1094/1/D6 1094/1/C6 1094/1/C6 —	If okay return to step 1
3	"BATTERY LOW" displayed	Battery Backup a. Battery below 2.4V b. Battery Test Circuit	4.2.3	 BT1, CR4, 5 U27, CR6	 1094/1/A3 1094/2/A3	If okay return to step 2
4	Keyboard has no effect	Keyboard a. ♪ key b. LCL key c. Keyboard d. Keyboard decoder	 4.3.2 4.3.2 4.3.2 4.3.2	 Keyboard Keyboard Keyboard U6,7	 Front panel Front panel 0921/1/B4 0921/1/A3-6	If okay return to step 2
5	Cannot recall stored settings	Stored Settings a. Battery backup b. Reset	4.2.3	 BT1, U12 U27, CR18, 19	 1094/1/A3-4 1094/2/A3	If okay return to step 2
6	Won't work on GPIB	GPIB a. Address switch b. Remote indicator c. Command recall	 4.2.1.8 4.2.2 4.2.2	 SW1, U5 U6-8 U6-8	 1094/1/C5 1094/1/C3 1094/1/C3	If okay return to step 2
7	Keyboard will not work with unit on GPIB	Local Lockput a. Verify remote indicator (R) not displayed b. Verify local lockout not set		 LCL key GTL command	 Front panel GPIB	If okay return to step 6

Table 6-2. Troubleshooting (Continued)

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
8	No or incorrect output at FUNC OUT (output on)	Test Connector: See Remarks				RESET instrument, with output on. If bad refer to:
		a. J23 pin 11 VCGTST = 0.0 ± 0.1 Vdc			0920/3/B1	step 8.1
		b. J23 pin 9 DCCOMP = 0.0 ± 5.0 Vdc			0920/3/B1	step 8.2
		c. J23 pin 7 TRITST = 0.0 ± 0.1 Vdc			0920/3/B1	step 8.3
		d. J23 pin 13 AMPLDC = 5.0 ± 0.2 Vdc			0920/3/B1	step 8.5
		e. J23 pin 1 PATEST = 0.0 ± 0.1 Vdc			0920/3/B1	step 8.6 If okay go to step 8.7
8.1	No output or incorrect frequency	VCG				
		a. SH0 (FRQ input)	4.2.5.3	U15-19, C28	1094/2/C2	
		b. VCG Amp & Compensation	4.4.1	U1-2, CR1-2	0920/1/C4	
		c. Curent Sources	4.4.1	U2-3, Q1, CR4-6	0920/1/C4	
8.2	High frequency incorrect, sine distortion excessive at low frequencies or no output.	Frequency Compensation				
		a. DC Amplifier	4.4.5	U7-8, C17,58	0920/2/C6	
		b. High Frequency Comp	4.4.5	U1, U7-8, Q2-3, CR15-16	0920/2/C6	
8.3	Sine distortion excessive, no output, or no sync output	Main Generator				
		a. Current Switch	4.4.2	Q4-5, CR17-20	0920/2/D4	
		b. Switch Buffer	4.4.2	Q6-7, CR21-23	0920/2/C4	
		c. Comparator	4.4.2	Q8-12, CR24-31	0920/2/C3	
		d. Square Buffer	4.4.2	Q13-14, CR32-34	0920/2/C2	
		e. Triangle Buffer	4.4.2	Q15-17, CR66	0920/2/C1	
		f. Frequency Range Switches	4.4.3	Q18-21, CR35-43, C43-47, 50, 52, 54	0920/2/B2-4	
		g. Sync Driver	4.4.6	Q26-27, CR52-53	0920/3/C3-D3	
8.4	No output, or frequency incorrect below 100 Hz	Capacitance Multiplier	4.4.4	U8-11, C40	0920/2/A6-7	
8.5	Excessive sine distortion and amplitude errors, or not output	Amplitude Control				
		a. SH1 (AMP)	4.2.5.3	U15-19, C32	1094/2/C2	
		b. Sine Converter	4.4.8	U11-12, Q22-23, R145	0920/3/C4-6	
		c. XY Multiplier	4.4.9	U17-19, CR59-62	0920/4/A5-8	
8.6	Offset Errors or no output	Preamplifier	4.4.10	U15, Q28-29, CR54	0920/4/C5-7	
8.7	Output offset or no output	Output				
		a. SH2 (OST)	4.2.5.3	U15-18,20, C36	1094/2/C2	
		b. Offset	4.4.9	U17	0920/4/B5	
		c. Output Amplifier	4.4.11	U16, Q30-37, CR55-58	0920/4/C1-5	
		d. Fuse and Fuse Sense	4.4.12.2	U20, F1	0920/4/B1-2	
		e. Overvoltage Sense	4.4.12.1	U20, CR63-65	0920/4/B4	
		f. Output Attenuator	4.4.12.3	Q38-41, K1-3	0920/4/B1-2	

Table 6-2. Troubleshooting (Continued)

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
9	No triangle out	Triangle Level	4.4.8	U12, Q24-25	0920/3/B5-6	If okay return to step 8.3
10	No square out	Square				
		a. Square Logic	4.4.8	U13-14	0920/3/B5-6	If okay return to step 8.3d
		b. Square Shaper	4.4.8	U12, CR45-51	0920/3/A3-4	
11	Trigger or gated mode error	Trigger Circuit				
		a. SH3 (TRL)	4.2.5.3	U15-18,20, C40	1094/2/B2-3	If okay return to step 8.1c
		b. Trigger Level Amplifier	4.4.1	U2	0920/1/B6	
		c. Trigger Comparator	4.4.7	U4, CR9-11	0920/1/B5	
		d. Mode Logic	4.4.7	U5-6, CR7-8,12-14	0920/1/B4	
12	No burst or incorrect burst count	Burst Counter				
		a. Auxiliary Buffers	4.2.4.3	U28-29	1094/2/B6-7	If okay return to step 10
		b. Auxiliary Connectors	—	cables	connectors	
		c. TRIG IN Jumpers	4.4.7	E13-E14	0920/1/A4	
		d. Program Decode	4.5.1	U1	0978/1/C7	
		e. Program Registers	4.5.1	U2-7	0978/1/C3-6	
		f. Burst Mode Logic	4.5.2	U8, U15	0978/1/A6	
		g. Preset Counter	4.5.2	U9-U13	0978/1/B2, C6	
13	Internal Trigger does not function or is inaccurate	Internal Synthesizer				
		a. Trig Select Switch	4.5.3.3	U38, U5, U36	0978/3/C7-5	
		b. Synthesizer Frequency dividers	4.5.3.3	U31-U36, U2, U7	0978/3/A7-D7	
		c. VCO (Synthesizer) Output	4.5.3.2	U26, Q3, U25	0978/2/B3-4	
		d. Level Translator	4.5.3.2	U24	0978/2/B5	
		e. Loop Filter	4.5.3.2	U23	0978/2/B6	
		f. PLL Chip	4.5.3.2	U21, VR2	0978/2/B8	
		g. VMP	4.5.3.2	U27-30	0978/2/B1-2	
		Internal Reference				
		a. Reference Dividers	4.5.3.1	U18-U20	0978/2/D1-2	
		b. Ref. Select Switch	4.5.3.1	U17	0978/2/D4	
		c. Ref. Buffer	4.5.3.1	U16, VR1	0978/2/D4	
		d. Ref. Oscillator	4.5.3.1	Q1, Q2, Y1	0978/2/D5-7	
14	Synthesized Frequency Inaccurate in Mode (4)	Internal Synthesizer				
		a. Synthesizer Output	4.5.3.2	U26, Q3, U25	0978/2/B3-4	
		b. Synth. Freq. Divider Out.	4.5.3.3	U31-U36, U2, U7	0978/3/A7-D7	
		Main Loop Select Logic				
		a. ϕ Lock Selector	4.5.4	U37	0978/3/C5	
		b. Main Loop $\div 2$	4.5.4	U40	0978/3/C4	
		Main Loop				
		a. ϕ Ref. Inputs	4.5.4	U40-U41	0978/3/C3-4	
		b. Main Loop Filter	4.5.2	U43-U45	0978/3/C3	
		c. Main Loop Control	4.5.2	U7	0978/1/C3	
		d. VCG Summing Node	4.5.2	U47, U48	0978/3/C1	
		e. Main Loop Lock Detector	4.5.2	U46	0978/3/B2	

Table 6-2. Troubleshooting (Continued)

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
15	Will not lock to an External Reference	TTL Reference Operation				
		a. Reference Select Logic	4.5.3.1	U17, U5	0978/2/D4	
		b. Ext. Ref. Buffer	4.5.3.1	U16, VR1, P13	0978/2/C5	
		Zero Reference Operation				
		a. Reference Select Logic	4.5.3.1	U17, U5	0978/2/D4	
		b. Ext. Ref. Buffer	4.5.3.1	U16, VR1, P13	0978/2/C5	
		TTL Lock				
		a. Reference Select Logic	4.5.3.1	U17, U5	0978/2/D4	
		b. Main Loop ϕ Select	4.5.4	U37, U5	0978/3/C6	
		Zero Lock				
		a. Reference Select Logic	4.5.3.1	U17, U5	0978/2/D4	
		b. Main Loop ϕ Select	4.5.4	U37, U5	0978/3/C6	
16	"LOOP NOT LOCKED" Displayed	Main Loop Status				
		a. Loop Inputs	4.5.4	U40, U41	0978/3/C4	
		b. Loop Filter Control	4.5.4	U43-U45	0978/3/C4	
		c. Lock Detector	4.5.5	U46	0978/3/B2	
		d. VCG Summing Node	4.5.4	U47, U48	0978/3/C1	
		e. Mode Programming		—	FRONT PANEL	
17	No Ref. Out	Driver Circuits				
		a. Output Buffer	4.5.6	Q4, Q5	0978/3/A4	
		b. Ref. Out. Select Logic	4.5.3.3	U39, U5	0978/3/B6	
		c. Output Connections		W16, FRONT PANEL	0978/3/A3	
18	5th Frequency Digit will not change in Mode (4)	Internal Synthesizer				
		a. VMP Circuit	4.5.3.2	U27-U30, U22	0978/2/B2	
		b. VMP Programming	4.5.3.2	U29, U6	0978/2/B2	

Table 6-3. Function Generator Board Voltages (Reset Condition)

Circuit	Control Voltages	Circuit Voltages
VCG and trigger level	$\overline{OVR}$ = TTL high (J9-19) $\overline{FR5}$ = TTL high (J9-10) FRQ = 1.00V (J9-1) TRL = +4.25V (J9-4)	TLO = +1.5V (U2-7) THC = +1.2V (U3-9) VCV = −0.4V (E10) VCGTST = 0.00 Vdc (J23-11)
Frequency compensation	$\overline{FR7}$ = TTL high (J9-12) $\overline{FR6}$ = TTL high (J9-11) $\overline{FR5}$ = TTL high (J9-10) $\overline{DCA}$ = TTL low (J9-18)	DC COMP = 0 ± 5V (U7-14)

Table 6-3. Function Generator Board Voltages (Reset Condition) (Continued)

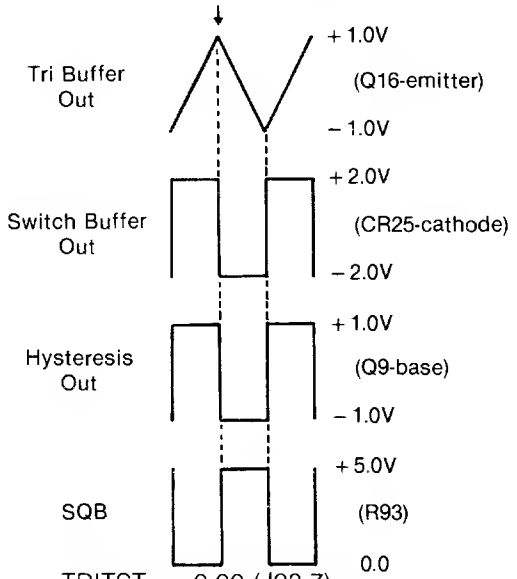
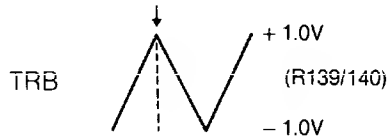
Circuit	Control Voltages	Circuit Voltages
Generator loop		 TRITST = 0.00 (J23-7) DC COMP = 0 ± 5V (J23-9)
Frequency range	$\overline{FR3}$ = TTL high (J9-8) $\overline{FR4}$ = TTL low (J9-9) $\overline{FR5}$ = TTL high (J9-10) $\overline{FR6}$ = TTL high (J9-11)	
Capacitance multiplier	$\overline{FR0}$ = TTL high (U10-9) $\overline{FR1}$ = TTL high (U10-8) $\overline{FR2}$ = TTL low (U10-1) $\overline{CPM}$ = TTL high (U10-16)	
Trigger circuit	+TR = TTL high (J9-22) −TR = TTL low (J9-21) MC0 = TTL low (J9-16) MC1 = TTL low (J9-17)	TLO = +1.5V (R29) THC = +1.2V (CR14-cathode) 
Function select	SQR = TTL low (U14-1) $\overline{SQR}$ = TTL low (U14-10) PLS = TTL low (U14-2) $\overline{PLS}$ = TTL low (U14-5) EXW = TTL low (U13-12) $\overline{SIN}$ = TTL low (R141) $\overline{TRI}$ = TTL high (R149) $\overline{RCT}$ = TTL high (R170)	
X-Y multiplier and offset		OST = +5.00V (R235) Amp out = 0.0 Vdc (U17-8) AMP = +5.00V (R266) AMPLDC = +5.00V (J23-13)

Table 6-3. Function Generator Board Voltages (Reset Condition) (Continued)

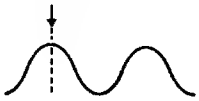
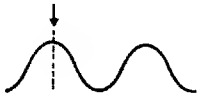
Circuit	Control Voltages	Circuit Voltages
Preamplifier		Preamp out  +0.75 CR54-anode) −0.75 PATEST = 0.0 Vdc (J23-1)
Output amplifier		Off amp out = 0.0 Vdc (R207) Preamp out  +0.75 (R209) −0.75 PATEST = 0.0 Vdc (J23-1) Out amp out  +5.0V (R231/232) −5.0V
Output protection	FUB = TTL low (J9-34) OAP = TTL low (J9-33) OA0 = TTL low (J9-13) OA2 = TTL low (J9-15)	Fuse sense input  +5.0V (F1) −5.0V

Table 6-4. Frequency Truth Table

Frequency Range	FR0	FR1	FR2	FR3	FR4	FR5	FR6	FR7	CPM	OVR	DCA
10.0 – 99.9 mHz	1	1	1	0	1	1	1	1	0	1	1
100 – 999 mHz	0	1	1	0	1	1	1	1	0	1	1
1.00 – 9.99 Hz	1	0	1	0	1	1	1	1	0	1	1
10.0 – 99.9 Hz	1	1	0	1	1	1	1	1	0	1	1
100 – 999 Hz	1	1	0	0	1	1	1	1	1	1	0
1.00 – 9.99 kHz	1	1	0	1	0	1	1	1	1	1	0
10.0 – 99.9 kHz	1	1	0	1	1	0	1	1	1	1	0
100 – 999 kHz	1	1	0	1	1	1	0	1	1	1	0
1.00 – 9.99 MHz	1	1	0	1	1	1	1	0	1	1	0
10.0 – 12.0 MHz	1	1	0	1	1	1	1	0	1	0	0

Table 6-5. Output Relay Truth Table

Condition	OA0	OA2	OA1
Ampl + |Ofst| > 1.00V, Output On	1	0	1
Ampl + |Ofst| ≤ 1.00V, Output On	1	1	0
Output Off, Hi Z (~539 kΩ)	0	0	1
Output Off, Lo Z (~55.6Ω)	0	1	0

Table 6-6. Function Truth Table

Function	$\overline{SIN}$	$\overline{TRI}$	$\overline{RCT}$	SQR	$\overline{SQR}$	PLS	$\overline{PLS}$	EXW	
Sine	0	1	1	0	0	0	0	0	∿
Triangle	1	0	1	0	0	0	0	0	∿
Square	1	1	0	1	0	0	0	0	⊓
Sqr Comp	1	1	0	0	1	0	0	0	⊓
DC	1	1	1	0	0	0	0	0	⎓
Ext Width	1	1	0	0	0	0	0	1	

Table 6-7. Mode Truth Table

Mode	MC0	MC1	
Cont	0	0	
Trig	1	0	
Gate	1	1	(Includes Burst Mode)

Table 6-8. Trigger Truth Table

Trigger	+TR	-TR	
+ (Rising)	1	0	⊣
− (Falling)	0	1	⊢
Man Trig	1	1	

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

7.2 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, errata pages are prepared to summarize the changes made and are inserted inside the shipping carton with this manual. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit, and, if applicable, the function performed.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

DRAWING	DRAWING NUMBER
Instrument Schematic	0004-00-0180
Instrument Parts List	1000-00-0185
Chassis Assembly	0102-00-1648
Chassis Parts Lists	1101-00-1648
Front Panel Assembly	0102-00-1003
Front Panel Parts List	1101-00-1003
Display Schematic	0103-00-0921
Display Assembly	1100-00-0921
Display Parts List	1100-00-0921
Function Generator Schematic	0103-00-0920
Function Generator Assembly	1100-00-0920
Function Generator Parts List	1100-00-0920
Microprocessor/Power Supply Schematic	0103-00-2202
Microprocessor/Power Supply Assembly	1100-00-2202
Microprocessor/Power Supply Parts List	1100-00-2202
Prom Package	1109-00-0021
Synthesizer Board Schematic	0103-00-0978
Synthesizer Board Assembly	1100-00-0978
Synthesizer Board Parts List	1100-00-0978
Rear Panel Assembly	0102-00-0924
Rear Panel Parts List	1101-00-0924

DRAWING	DRAWING NUMBER
Rack Adapter Assembly	0102-00-1043
Rack Adapter Parts List	1101-00-1043
Dual Rack Mount Assembly & Parts List	0102-00-1041
Rack Slide Assembly & Parts List	0102-00-1042
Option 002 Schematic & Parts List	0103-00-1010

REV	ECN	BY	DATE	APP
/	3369 CLASS III	SC	9/2/82	
A	# 3904	SC	7-26-83	

A5 REAR PANEL ASSY

J2 — IEEE - 488

1	D101
2	D102
3	D103
4	D104
5	EOI
6	DAV
7	RFD
8	DAC
9	IFC
10	SRQ
11	ATN
12	
13	D105
14	D106
15	D107
16	D108
17	REN
18	GND
19	GND
20	GND
21	GND
22	GND
23	GND
24	GND

J18 — AC POWER RECP
100 - 120V - ½A SB
220 - 242 ¼A SB
F1

T1 — 1204-00-0049
W1 — P1 — J1
15 VAC
15 VAC
15 VAC
15 VAC
GND
5 VAC
5 VAC

TEST CONNECTOR
J8: E, ADR 15, GND, ADR 14, A5, A1DR 13, GND, ADR 12, NMI, ADR 11, GND, ADR 10, GND, ADR 9, GND, ADR 8, GND, AD7, GND, AD6, GND, AD5, TEST, AD4, GND, AD3, +5V, AD2, N.C., AD1, N.C., AD0, GND, R/W

A6 μ PROC/POWER SUPPLY BOARD

A2 FRONT PANEL ASSY

J7 P7 — W4 — J11

1	+45V
2	GND
3	+5V
4	+5V
5	+5V
6	+5V
7	KYBD
8	PORT
9	PORT 16
10	DISP/
11	GND
12	AD4
13	AD3
14	AD2
15	AD1
16	AD0
17	ADR 3
18	ADR 2
19	ADR 1
20	ADR 0
21	GND
22	DATA 7
23	DATA 6
24	DATA 5
25	DATA 4
26	DATA 3
27	DATA 2
28	DATA 1
29	DATA 0
30	GND
31	GND
32	GND
33	+15V

A3 DISPLAY BOARD 1100 - 00 - 0921

A4 CABLE INTERFACE BOARD

MODEL 278 ONLY

P13 J13 — W16 — W18 — J24 REF OUT
P13 J13 — W17 — W19 — J25 REF IN

P12 J12 — W9 — J19 FUNC OUT
P12 J12 — W10 — J20 SYNC OUT
P12 J12 — W11 — J21 TRIG IN
P12 J12 — W12 — J22 VCG IN

J3 P3 — W2 — J6 P6
J4 P4 — W13 — J5 P5
W14
J16 P16 — J17 P17

A10 AUXILLARY FUNCTION BOARD

E1
E2
E3
E4

J15 P15 — W15 — J14 P14

1	GND
2	VCGI
3	GND
4	VCGO
5	GND
6	GND
7	TRIG
8	GND
9	TRGO
10	GND
11	PLSI
12	GND
13	SGS
14	GND

J10 P10 — W3 — J9 P9

A7 FUNCTION GENERATOR BOARD

A8 OUTPUT FUSE BOARD

FUNC OUT E1 E2 — W5
SYNC OUT E3 E4 — W6
TRIG IN E5 E6 — W7
VCG IN E7 E8 — W8

TEST CONNECTOR
J23: PA TEST, +15 VT, -15 VT, GND, +5 VT, GND, TRI TST, GND, DC COMP, GND, VCG TST, GND, AMP LDC, GND

A1 CHASSIS ASSY

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN FN AQUINO	DATE 9/29/80	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL —	PROJ ENGR RBG	7/1/82	TITLE SCHEMATIC INSTRUMENT	
FINISH WAVETEK PROCESS —	RELEASE APPROV BG			
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030			
	DO NOT SCALE DWG		MODEL NO 270, 271, 278	DWG NO. 0004-00-0180 REV A
	SCALE		CODE IDENT 23338	SHEET 1 OF 1

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT	0004-00-0180	WVTK	0004-00-0180	1
NONE	FINAL CAL PROCEDURE	0006-00-0185	WVTK	0006-00-0185	1
NONE	MODEL 278 ACCEPTANCE TEST PROCEDURE	0007-00-0185	WVTK	0007-00-0185	1
NONE	PCA, FUNCTION GEN	270-0920	WVTK	1100-00-0920	1
NONE	PCA, DISPLAY	270-0921	WVTK	1100-00-0921	1
NONE	PCA, SYNTHESIZER B0	270-0978	WVTK	1100-00-0978	1
NONE	PCA, CABLE INTERFACE	270-1006	WVTK	1100-00-1006	1
NONE	ASSY MICRO-PROC/GPIB BOARD	1100-00-2202	WVTK	1100-00-2202	1
NONE	CHASSIS ASSY-271	271-0922	WVTK	1101-00-0922	1
NONE	ASSY, REAR PANEL	270-0924	WVTK	1101-00-0924	1
NONE	ASSY, FRONT PANEL-278	278-1003	WVTK	1101-00-1003	1
NONE	PROM PACKAGE	270-0021	WVTK	1109-00-0021	1
NONE	CHASSIS CABLE KIT	270-1004	WVTK	1207-00-1004	1
NONE	MODEL 278 INSTRUCTION MANUAL	MANUAL-278	WVTK	1300-00-0185	1
NONE	NUT, SPEED, SELF RETAIN	C7494-632-4	TINN	2800-09-0003	2

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	MODEL 278 12MHZ PROGRAMMABLE SYNTH-O	1000-00-0185	D
		PAGE 1	

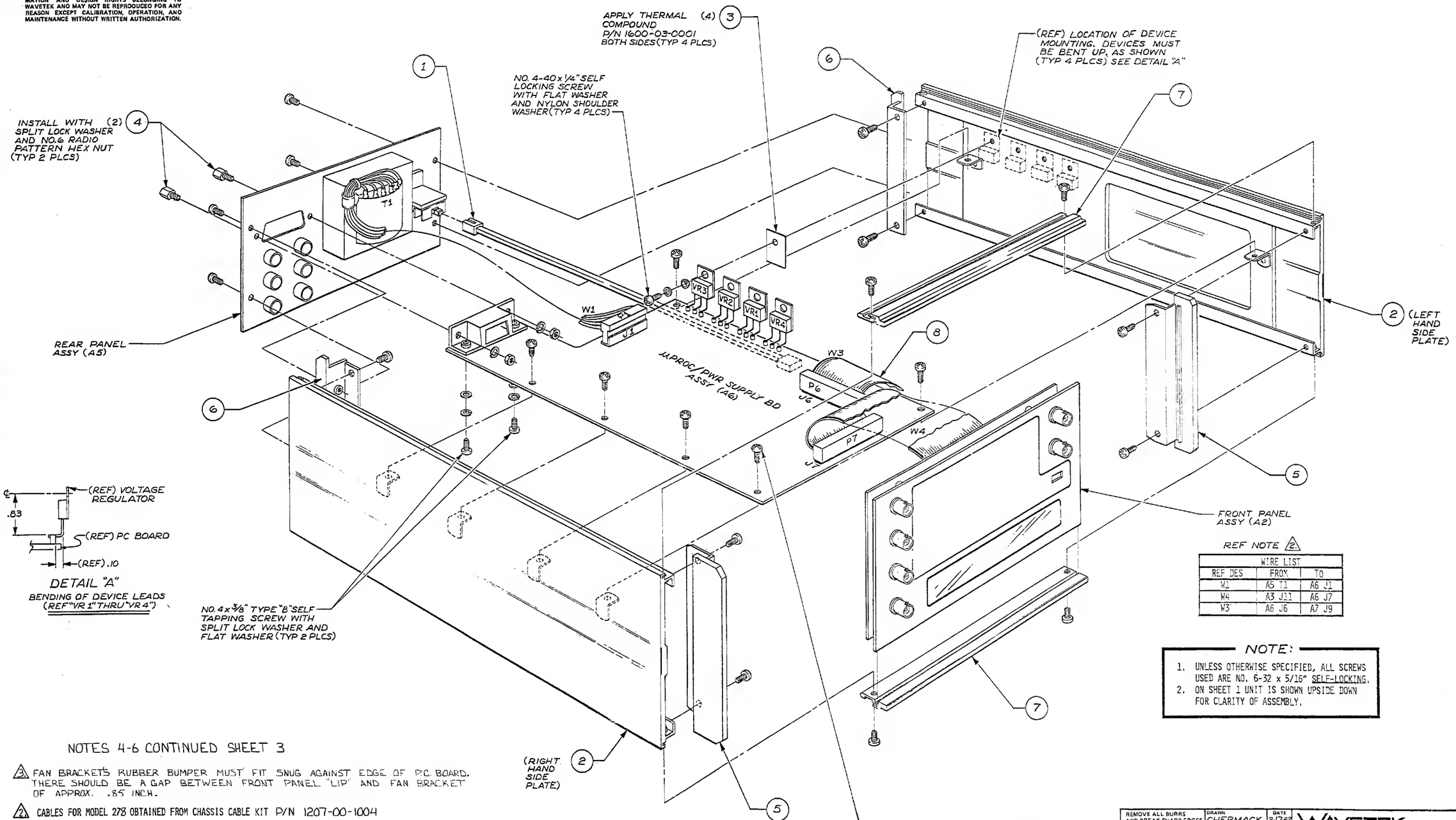
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	101-6F INSERT	101-6F	WVTK	3300-00-0013	1
NONE	CARTON 22X15 1/4X10 1/4, 200#, SINGLE, RSC	101-6A	WVTK	3300-01-0010	1
NONE	PWR CORD	17251	BELDN	6001-80-0005	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	MODEL 278 12MHZ PROGRAMMABLE SYNTH-O	1000-00-0185	O
		PAGE 2	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST MODEL 278 12 MHZ PROGRAMMABLE SYNTH-D FUNCTION GENERATOR
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 278 · DWG NO 1000-00-0185 · REV D
	SCALE		CODE IDENT 23338 · SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP
A	ECO # 82-010	MS	1/28/82	



REF NOTE (2)

WIRE LIST		
REF DES	FROM	TO
W1	A5 T1	A6 J1
W4	A3 J11	A6 J7
W3	A6 J6	A7 J9

NOTE:

1. UNLESS OTHERWISE SPECIFIED, ALL SCREWS USED ARE NO. 6-32 x 5/16" SELF-LOCKING.
2. ON SHEET 1 UNIT IS SHOWN UPSIDE DOWN FOR CLARITY OF ASSEMBLY.

NOTES 4-6 CONTINUED SHEET 3

(3) FAN BRACKET'S RUBBER BUMPER MUST FIT SNUG AGAINST EDGE OF P.C. BOARD. THERE SHOULD BE A GAP BETWEEN FRONT PANEL "LIP" AND FAN BRACKET OF APPROX. .85 INCH.

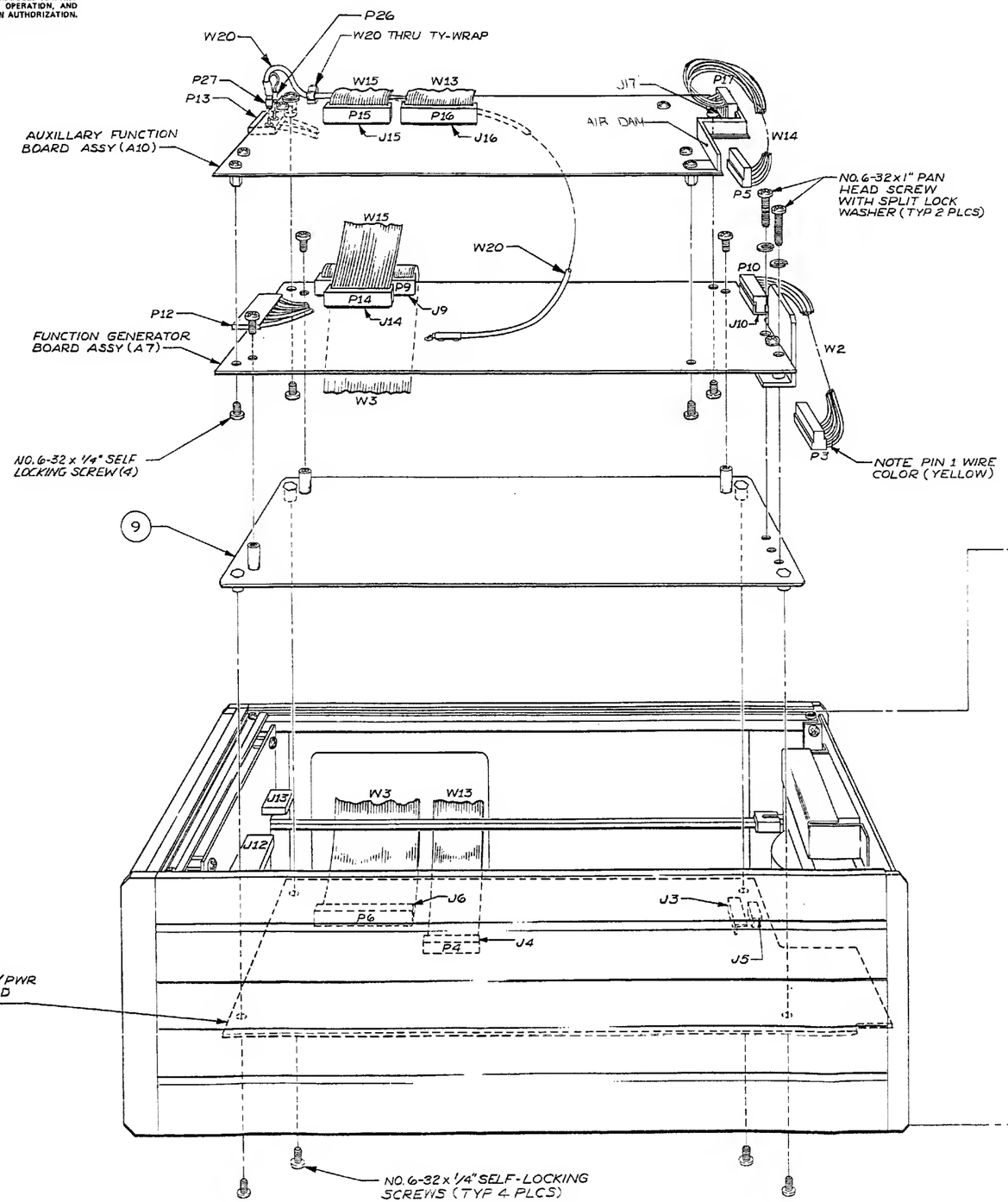
(2) CABLES FOR MODEL 278 OBTAINED FROM CHASSIS CABLE KIT P/N 1207-00-1004

1. FOR UNIT INTERCONNECTION SEE INSTRUMENT SCHEMATIC # 0004-00-0180.

NOTE: UNLESS OTHERWISE SPECIFIED

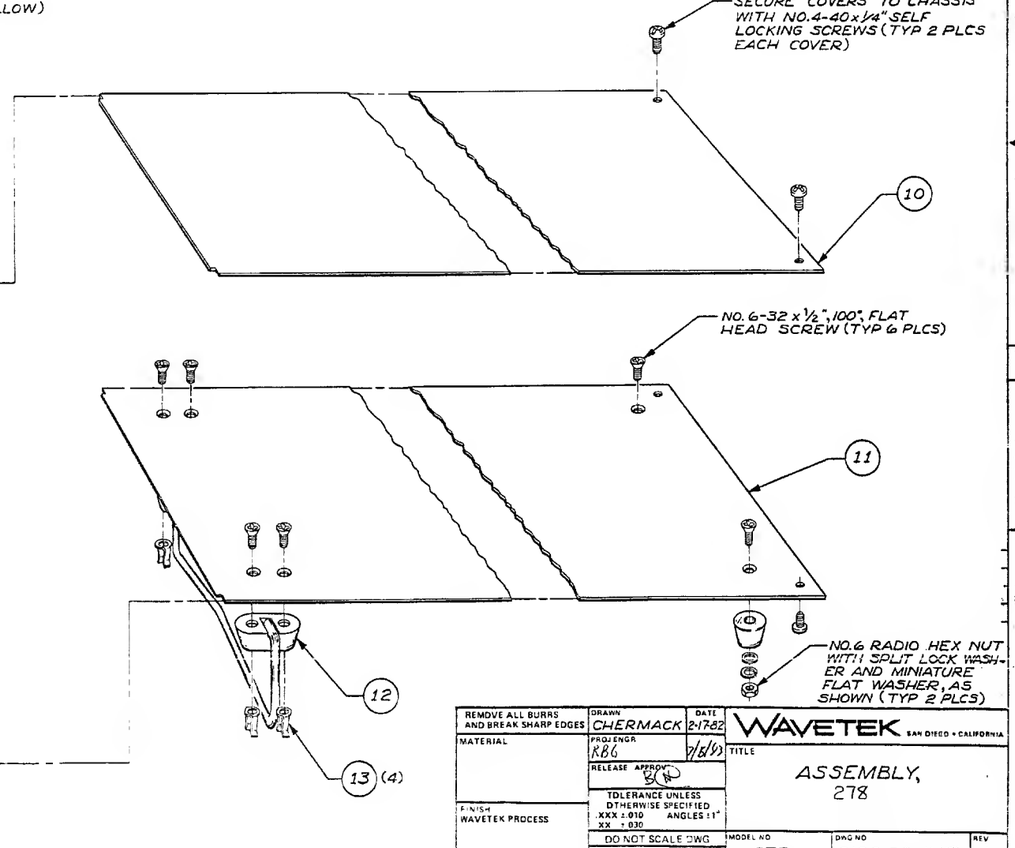
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 2-17-82	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR K86	7/15/82	TITLE ASSEMBLY, 278
	RELEASE APPROV BH		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO. 278	DWG NO. 0102-00-1648 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 4

REV	ECN	BY	DATE	APP



REF NOTE (2)

WIRE LIST		
REF DES	FROM	TO
W2	A6 J3	A7 J10
W3	A6 J6	A7 J9
W5,W6,W7,W8	A7	A4 J12
W16,W17	A10	A4 J13
W14	A10 J5	A6 J17
W13	A6 J4	A10 J16
W15	A7 J14	A10 J15
W20	A7 E15	A10 J26
	A7 E16	A10 J27

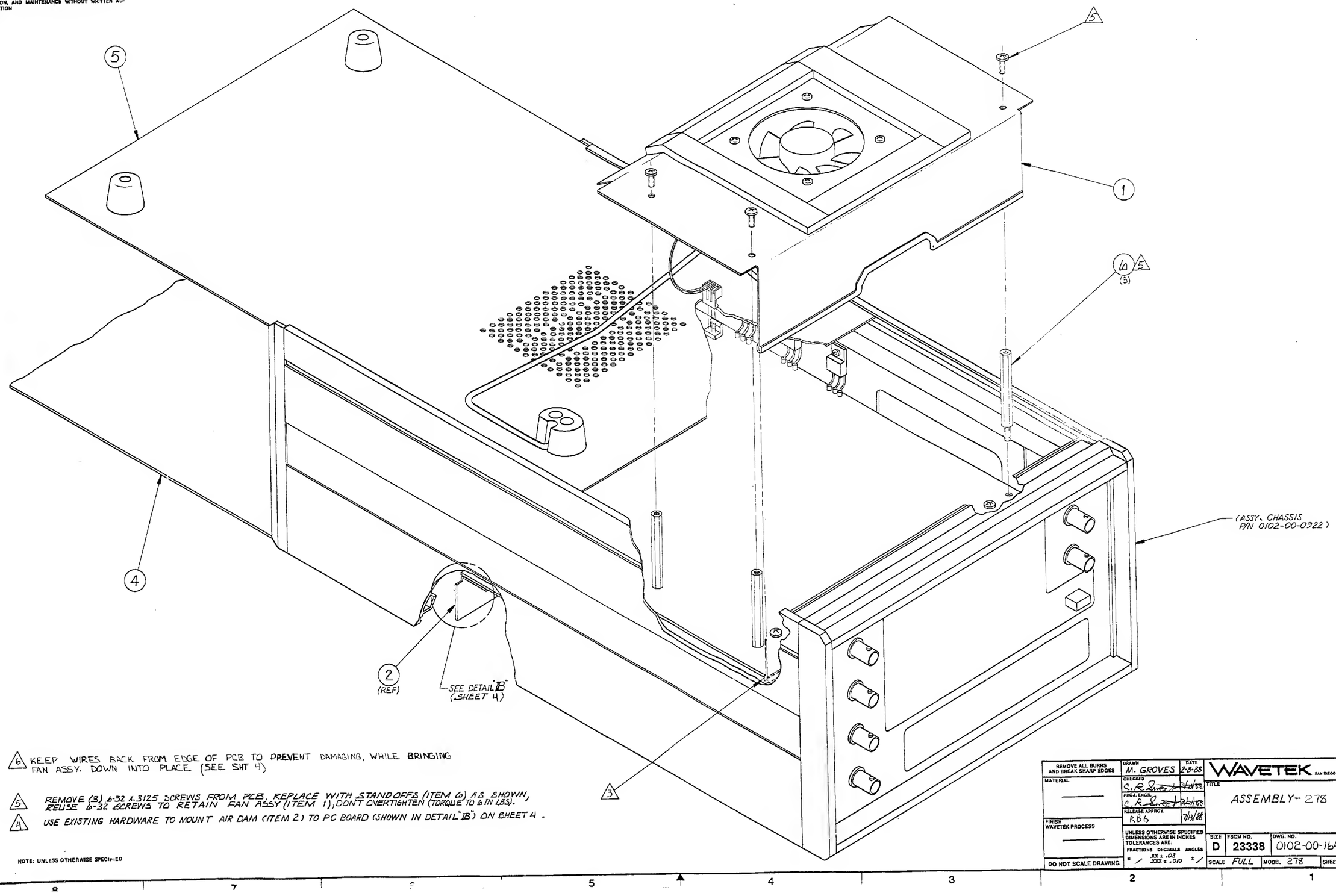


NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 2-17-82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/8/83	TITLE ASSEMBLY, 278
	RELEASE APPROVAL		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO 278 / DWG NO 0102-00-1648 / REV A
	SCALE NONE		CODE IDENT 23338 / SHEET 2 OF 4

BISHOP GRAPHICS/ACCUPRESS LAYOUT NO. A-3994

REV	ECO	BY	DATE	APP



6 KEEP WIRES BACK FROM EDGE OF PCB TO PREVENT DAMAGING, WHILE BRINGING FAN ASSY. DOWN INTO PLACE. (SEE SHT 4)

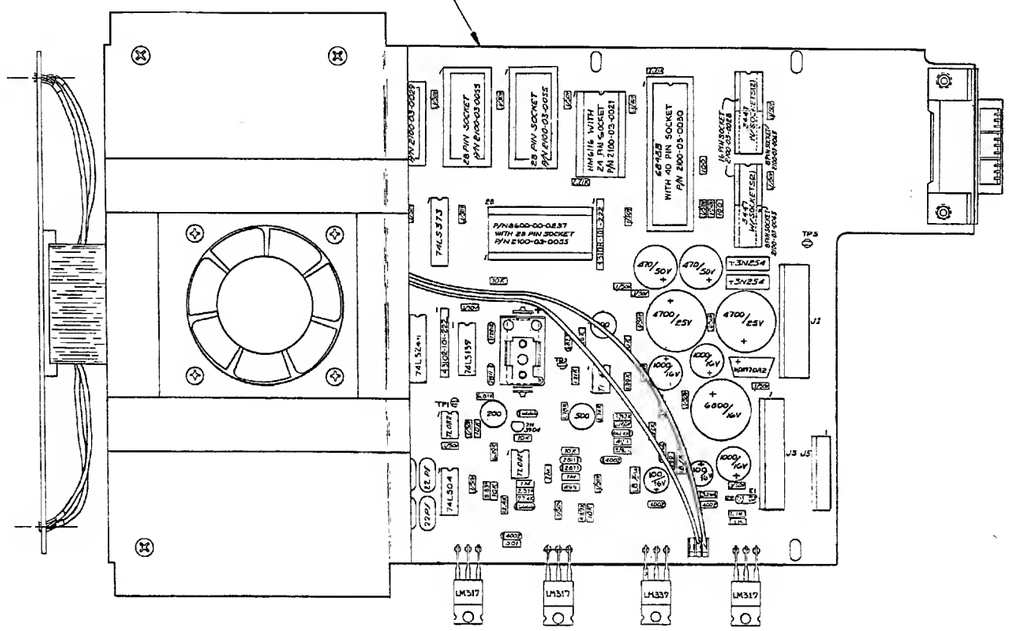
5 REMOVE (3) 6-32 X .3125 SCREWS FROM PCB. REPLACE WITH STANDOFFS (ITEM 6) AS SHOWN, REUSE 6-32 SCREWS TO RETAIN FAN ASSY (ITEM 1), DON'T OVERTIGHTEN (TORQUE TO 6 IN LBS).

4 USE EXISTING HARDWARE TO MOUNT AIR DAM (ITEM 2) TO PC BOARD (SHOWN IN DETAIL "B") ON SHEET 4.

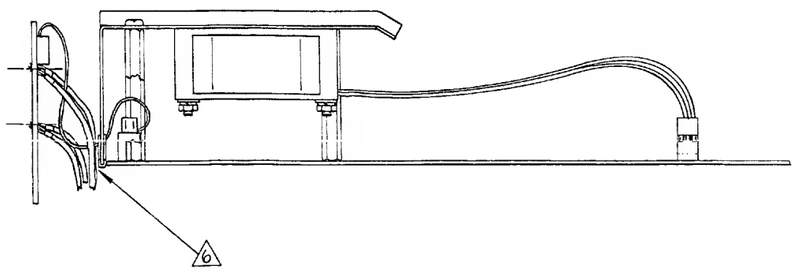
NOTE: UNLESS OTHERWISE SPECIFIED

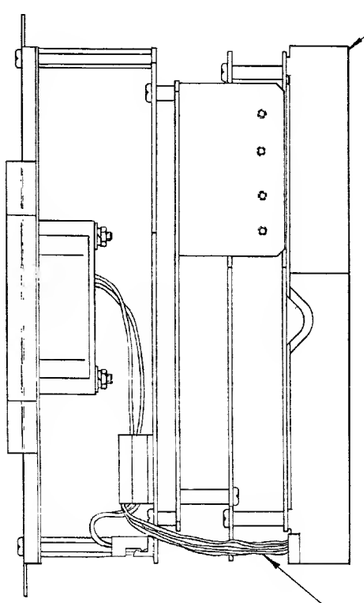
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN M. GROVES	DATE 2-8-88	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL ———	CHECKED C.R.	2/8/88	TITLE ASSEMBLY- 278
	PROJ. ENGR. C.R.	2/8/88	
FINISH WAVETEK PROCESS ———	RELEASE APPROV. R.B.G.	7/13/88	
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± 1/ DECIMALS XX ± .02 XXX ± .010 ANGLES ± 1/		SIZE D · FSCM NO. 23338 · DWG. NO. 0102-00-1648 · REV A · SCALE FULL · MODEL 278 · SHEET 3 OF 4

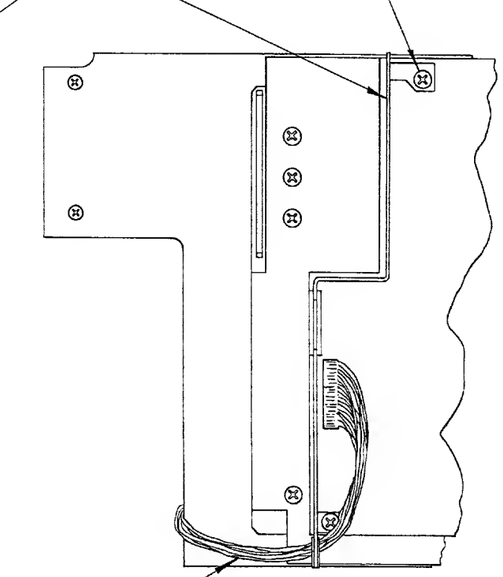
REV	ECO	BY	DATE	APP
	SEE SHEET 1			



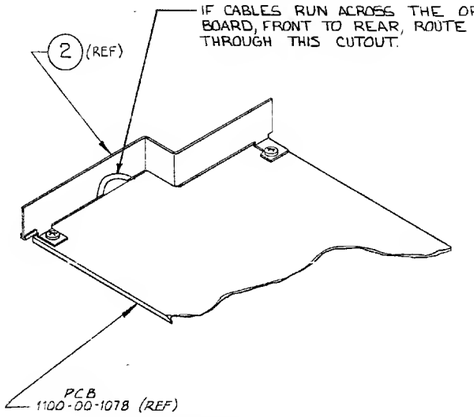
DETAIL "A"







DETAIL "B"



CLARIFICATION DETAIL
SCALE : NONE

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN M. GROVES	DATE 2-8-88	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED C.R. Swartz	2/14/88	TITLE ASSEMBLY- 278
	PROJ. ENGR. C.R. Swartz	2/14/88	
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± / DECIMALS XX ± .XXX ± ANGLES ± /		SIZE D · FSCM NO. 23338 · DWG. NO. 0102-00-1648 · REV A · SCALE FULL · MODEL 278 · SHEET 4 OF 4

REV	ECO	BY	DATE	APP

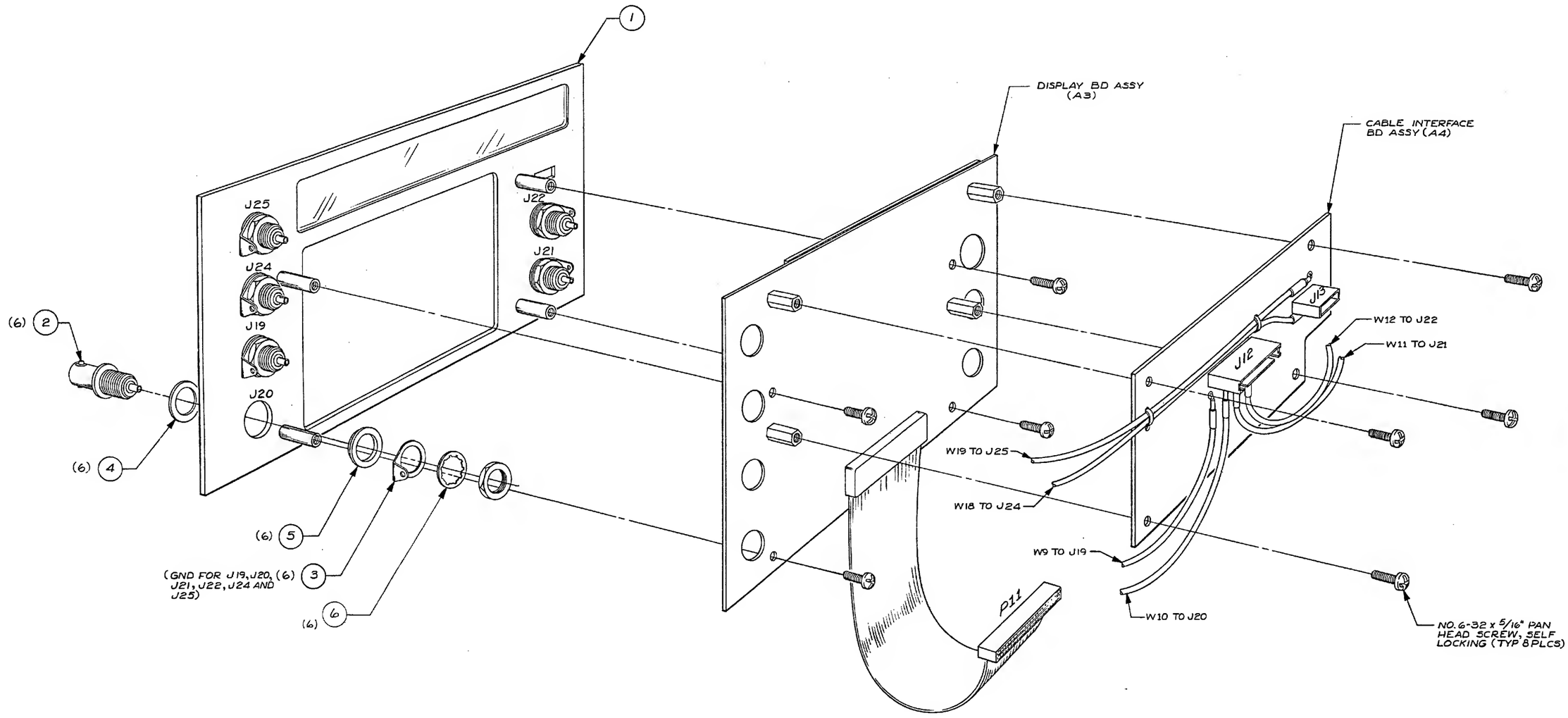
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG. CHASSIS-278	0102-00-1648	WVTK	0102-00-1648	1
NONE	PCA, FUNCTION GEN	270-0920	WVTK	1100-00-0920	1
NONE	PCA, SYNTHESIZER BD	270-0978	WVTK	1100-00-0978	1
NONE	ASSY MICRO-PROC/GPIB BOARD	1100-00-2202	WVTK	1100-00-2202	1
NONE	ASSY, REAR PANEL	270-0924	WVTK	1101-00-0924	1
NONE	ASSY, FRONT PANEL-278	278-1003	WVTK	1101-00-1003	1
NONE	PROM PACKAGE	270-0021	WVTK	1109-00-0021	1
NONE	ASSY, CHASSIS SUB 273-1655	273-2549	WVTK	1206-00-2549	1
NONE	ASSY, FAN	1206-00-3088	WVTK	1206-00-3088	1
NONE	ASSY, AIR DAM 271, 273, 278	1206-00-3114	WVTK	1206-00-3114	1
NONE	CHASSIS CABLE KIT	270-1004	WVTK	1207-00-1004	1
NONE	STANDOFF MALE/FEM, 1.687H, .250 HEX 6-32 THD.	1473-M03-F07-632	UNICP	2800-02-0039	3

WAVETEK PARTS LIST	TITLE CHASSIS ASSY-278	ASSEMBLY NO 1101-00-1648 PAGE 1	REV B

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE PARTS LIST CHASSIS ASSEMBLY
	PROJ. ENGR		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±		SIZE D FSCM NO. 23338 DWG. NO. 1101-00-1648 REV B SCALE MODEL 278 SHEET 1 OF 1

REV	ECN	BY	DATE	APP
/	3612 CLASS III	SC	11483	B.
B	#7841	M. C.	3-5-87 3/4/87	SS



WIRE LIST		
REF. DES.	FROM	TO
W9	A4 E1	J19
	A4 E2	J19
W10	A4 E3	J20
	A4 E4	J20
W11	A4 E5	J21
	A4 E6	J21
W12	A4 E7	J22
	A4 E8	J22
W19	A4 E9	J25
	A4 E10	J25
W18	A4 E11	J24
	A4 E12	J24

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERMACK	DATE 1-26-82	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/15/83	TITLE ASSEMBLY, FRONT PANEL (A2)
FINISH WAVETEK PROCESS	RELEASE APPROV D/M		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO 273, 275, 278. DWG NO 0102-00-1003 REV B
	SCALE NONE		COG IDENT 23338 SHEET 1 OF 1

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, FRONT PANEL	0102-00-1003	WVTK	0102-00-1003	1
1	ASSY, PANEL	270-1005	WVTK	1206-00-1005	1
2	CONN BNC	KC-7946	KING	2100-01-0002	6
3	SOLDER LUG	1497	SMITH	2100-04-0012	6
6	WASHER, 1/2 IN IT	1/2 IN IT WASHER	CMRCL	2800-24-0008	12
5	WASHER, SHOULDER	2668	SMITH	2800-27-0004	6
4	WASHER NYLON FLAT	2264-N-385	AMTOM	2800-28-0005	6

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	ASSY, FRONT PANEL-278	1101-00-1003	B
		PAGE 1	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST ASSY, FRONT PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± 010 ANGLES ± 1 .XX ± 030		
	DO NOT SCALE DWG	MODEL NO 278	DWG NO. 1101-00-1003 REV. B
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A27086

REV	ECN	BY	DATE	APP
A	#3904	SC	8-10-81	
/	4154 CLASS III	SC	2-6-84	

SEGMENT DRIVERS

U1 UCN4815A: DATA Ø–DATA 7, ADR Ø, STROBE, CE, OE → ANOO, ANODP, ANOF, ANOE, ANOD, ANOC, ANOB, ANOA

U2 UCN4815A: DATA Ø–DATA 7, ADR 1, STROBE, CE, OE → ANON, ANOM, ANOL, ANOK, ANOJ, ANOI, ANOH, ANOG

U5A LS04 (DISP)

U5B LS04 (BLANK)

C1–C5 .1/50V

R1 1K

DIGIT DRIVERS

U3 UCN4810A: DI, DSP, CLK, DO, OE → GRID 11, GRID12, GRID13, GRID 14, GRID 15, GRID 16, GRID 17, GRID 18, GRID 19, GRID 2Ø

U4 UCN4810A: DI, DSP, CLK, OE → GRID1, GRID2, GRID3, GRID4, GRID 5, GRID 6, GRID 7, GRID 8, GRID 9, GRID 1Ø

CR1, CR2 FD6666

R2 1K

C3, C4, C6, C7 .1/50V

FILAMENT DRIVER

+15V, C15 100/16V, C11 .1/50V, R6 10, R4 63.4K, R5 95.3K, CR3, CR4 FD6666(2), U8 NE555, C12 910PF, C13 .1/50V, C14 100/16V

VACUUM FLOURESCENT DISPLAY

V1 FG206A2: GRID 1–GRID 2Ø, FILA, FILA → ANOO, ANODP, ANOF, ANOE, ANOD, ANOC, ANOB, ANOA, ANON, ANOM, ANOL, ANDK, ANOJ, ANOI, ANOH, ANOG

J11 DISPLAY

1 +45V; 2 GND; 3; 4; 5; 6; 7 +5V; 8 KYBD; 9 BLANK; 10 DSP; 11 DISP; 12 GND; 13 AD4; 14 AO3; 15 AD2; 16 AD1; 17 AD Ø; 18 AOR3; 19 ADR2; 20 ADR1; 21 ADRØ; 22 GND; 23 DATA 7; 24 DATA 6; 25 DATA 5; 26 DATA 4; 27 DATA 3; 28 DATA 2; 29 DATA 1; 30 DATA Ø; 31 GND; 32 GND; 33 GND; 34 +15 V

C16, C17 .1/50V TO GND ON INTERFACE BD (A4); C9 100/16V

KEYBOARD

U6 74LS240: AD Ø, AD1, AD2, AD3, AD4 → AOR Ø, ADR1, ADR2, ADR3

C8 .1/50V; R3 10K SIP

KEYBOARD DECODER

U7 74LS145; C10 .1/50V

1. ALL CAPACITORS ARE SHOWN IN MICRO-FARADS.
3. ALL RESISTORS ARE SHOWN IN OHMS.
2. ALL DIODES ARE FD6666.
1. REFERENCE DESIGNATORS SHOWN ARE PARTIAL, PREFIX WITH ASSEMBLY REF DES (A3).

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS

DRAWN S.CHERMACK 8-17-81 | PROJ ENGR RB6 7/15/83 | RELEASE APPROV PAD

TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1

DO NOT SCALE DWG | SCALE

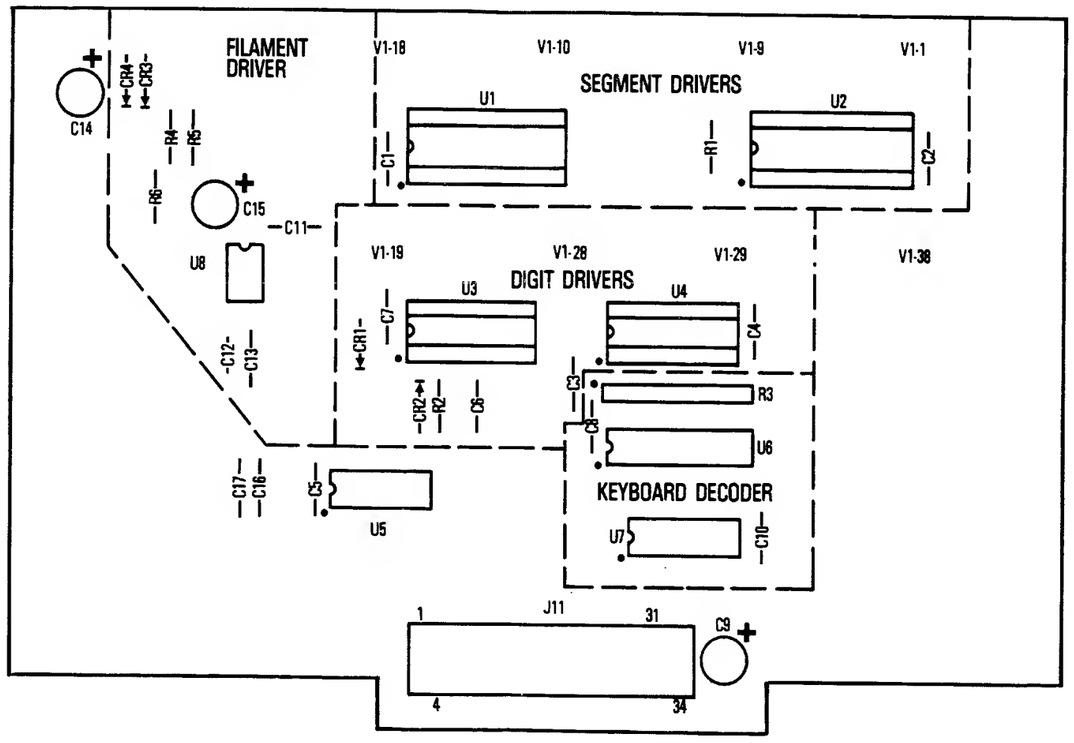
WAVETEK SAN DIEGO • CALIFORNIA

TITLE: SCHEMATIC, DISPLAY BOARD (A3)

MODEL NO 270 SERIES | DWG NO 0103-00-0921 | REV A

CODE IDENT 23338 | SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-2984



MADE FROM 0100-00-0921-3D

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: DISPLAY

MODEL NO	ASSY. NO.	REV
278	1100-00-0921	
CODE IDENT 23338	SHEET 1 OF 1	

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, DISPLAY	0101-00-0921	WVTK	D1D1-00-0921	1
NONE	SCHEMATIC, DISPLAY	0103-00-0921	WVTK	D103-00-0921	1
NONE	SPK ASSY, KEYBOARD	178/270-0939	WVTK	1206-00-0939	1
C1 C10 C11 C13 C16 C17 C2 C3 C4 C5 C6 C7 C8	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNO	1500-01-0405	13
C12	CAP, MICA, 910PF, 100V, 1%, RADIAL	DMI5-911F	ARCO	I500-19-I1D1	1
C14 C15 C9	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	ULB1V1D1M	NICH	I500-31-01D2	3
NONE	DISPLAY BOARD	270-0921	WVTK	1700-00-0921	1
NONE	SKT, IC, 22 PIN	D1L822P-108T	BURND	2100-03-0035	2
NONE	SOCKET, 18 PIN	D1LB18P-108T	BURND	2100-03-0050	2
V1	DISPLAY, FLOUR.	FG206A2	ITRON	2400-03-0009	1
NONE	STANDOFF, SWAGE .500 H, .250 HEX6-32, .062 MAT'L	1531B-1/2-11	USECO	2800-02-0003	4
R1 R2	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	2
R6	RES, MF, 1/8W, 1%, 10	RN55D10R0F	MEPCO	4701-03-1009	1
R4	RES, MF, 1/8W, 1%, 63.4K	RN55D-6342F	TRW	4701-03-6342	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, DISPLAY	1100-00-092I	A

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R5	RES, MF, 1/8W, 1%, 95.3K	RN55D-9532F	TRW	47D1-03-9532	1
R3	RES NETWORK 10K 2% 10PIN SIP BUSS	4310R-1D1-103	BOURN	4770-00-0008	1
CR1 CR2 CR3 CR4	DIODE 1N4148 COMPUTER, G/P, 75V, 200MA, SWITCHING	1N4148	FAIR	4807-02-6666	4
W4	ASSY, RIBBON CABLE	922522-34-02-4.5	A/P	6002-00-0009	1
U8	TIMING CIRCUIT, SILICON MONOLITHIC	LM555CN	NSC	7000-05-5500	1
U3 U4	DRIVER, 10 BIT SI, BIMOS	TL4810AN	TI	8000-48-1000	2
U1 U2	DRIVER, LTCH/SORC, BIMOS	UCN5815A	SPRAG	8000-48-1500	2
U5	INVERTER, HEX, TTL	74LS04	TI	8000-74-04I0	1
U7	CODR/DRV, BCD-DEC, TTL	74LS145	SIG	8007-41-4510	1
U6	BUF, OCT 3ST OUT, TTL	M74LS240P	MITSU	8007-42-40ID	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, DISPLAY	1100-00-0921	A

PAGE 2

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA DISPLAY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 278	DWG NO. 1100-00-0921 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A-3914

VCG & TRIGGER LEVEL

REV	ECN	BY	DATE	APP
A	# 3904	SC	7-27-83	
/	4144 CLASS III	SC	2-7-84	
B	ECN 4295	RO	9-14-84	
C	ECNS 4308 4336	RO	9-7-84	
D	# 8017	TC 3-6-87	3-6-87	SS
E	# 8419	TC 7-29-87	7/31/87	SS

VCG COMPENSATION
VCG AMPLIFIER
CURRENT SOURCES
+5V
+15 VR
DG211 U1D
R1 150K
R2 150K
OVR
DG211 U1C
R3 1M
FRS
FRQ
R4 4.99K
R5 4.99K
C1 .1
R7 3.57K
FREQ HI
R8 1K CW
C2 .1
VCG IN E7
GND E8
R6 10K
TL084 U2A
CR1 IN4148
CR2 IN4148
C3 .1
R10 1M
R11 100K CW
VCG ZERO
R9 2.49K
FREQ LO
R12 100K CW
R13 499K
R14 1K
C4 100 PF
TL084 U2D
R17 1K
CR3 IN4148
LO SYM
R15 100K CW
R16 1M
R19 4.99K
C124 .1
CR4 IN9338
HI SYM
R23 100 CW
R22 1K DIP
R24 23.7K
U3B CA3096A
R22 1K DIP
C6 220 PF +I
VCG JUMPER E9 E10 E11
VCGO VCGI
R18 1K
C5 100 PF
TL084 U2C
CR5 IN4148
R20 1K
CR6 IN9338
C125 .1
R21 4.99K
R301 10K
VCV
VCGTST
R22 1K DIP
CR7 FD777 ⚠6
-I
THC
U3A
Q1 2N3903
SS
R22 1K DIP
R22 1K DIP
R22 1K DIP
R22 1K DIP
TP1 TP2 TP3 TP4
-15 VR
+5V
+15V

TRIGGER LEVEL AMPLIFIER
-15VR
R25 30.1K
R26 20K
R27 4.99K
R28 4.99K
TL084 U2B
TRL
TLO
C7 .1
R29 4.99K
C24 .1
R303 2.49K
C9 .1
C10 .1
R304 20K
C12 .1
C13 .1
MCØ
U5A 74F00
R36 2.49K
CR8 FD777 ⚠6
TRN
SQB
U5B 74F00
C126 1.5pF
U5D 74F00
MCI
U5C 74F00
TRIG JUMPER E12 E13 E14
TRGO
TRGI
U6A 74F74
U6B 74F74
CR9 IN4148
R33 100K
-TR
CR12 IN4148
CR13 IN4148
CR14 IN4148
C8 10 pf
R30 3.32 K
R31 7.5K
TRIG IN E5
GND E6
U4 NE529
R32 2.49K
CR10 IN4148
CR11 751A
R37 8.25K
+TR
R35 100K
R305 20K
C127 1.5pf
R34 2.49K
C11 .1
-15V

TRIGGER COMPARATOR & SLOPE LOGIC
MODE LOGIC

LAST USED	NOT USED
R303	R143, R144
C126	
CR68	
U20	
Q41	
K3	
E16	
TP1	

9. # NOMINAL VALUE CALLED OUT ON PARTS LIST.
⚠4 MATCH SET RESISTORS (3) P/N 4789-00-0043 (REF R113, R114, R115)
⚠4 MATCHED SET CAPACITORS (3) P/N 1509-80-0008 (REF C50, C52, C54)
⚠6 MATCHED PAIR FD777 DIODES P/N 4898-00-0004 (REF CR8, CR7)
⚠5 MATCHED SET .1% RESISTORS (4) P/N 4701-02-7500 (REF R194, R198, R189, R192)
4. ALL CAPACITORS ARE IN MICRO-FARADS.
3. ALL DIODES ARE FD6666
2. ALL RESISTORS ARE IN OHMS.
1. REFERENCE DESIGNATORS SHOWN ARE PARTIAL, PREFIX WITH ASSEMBLY REF DES (A7)
NOTE: UNLESS OTHERWISE SPECIFIED

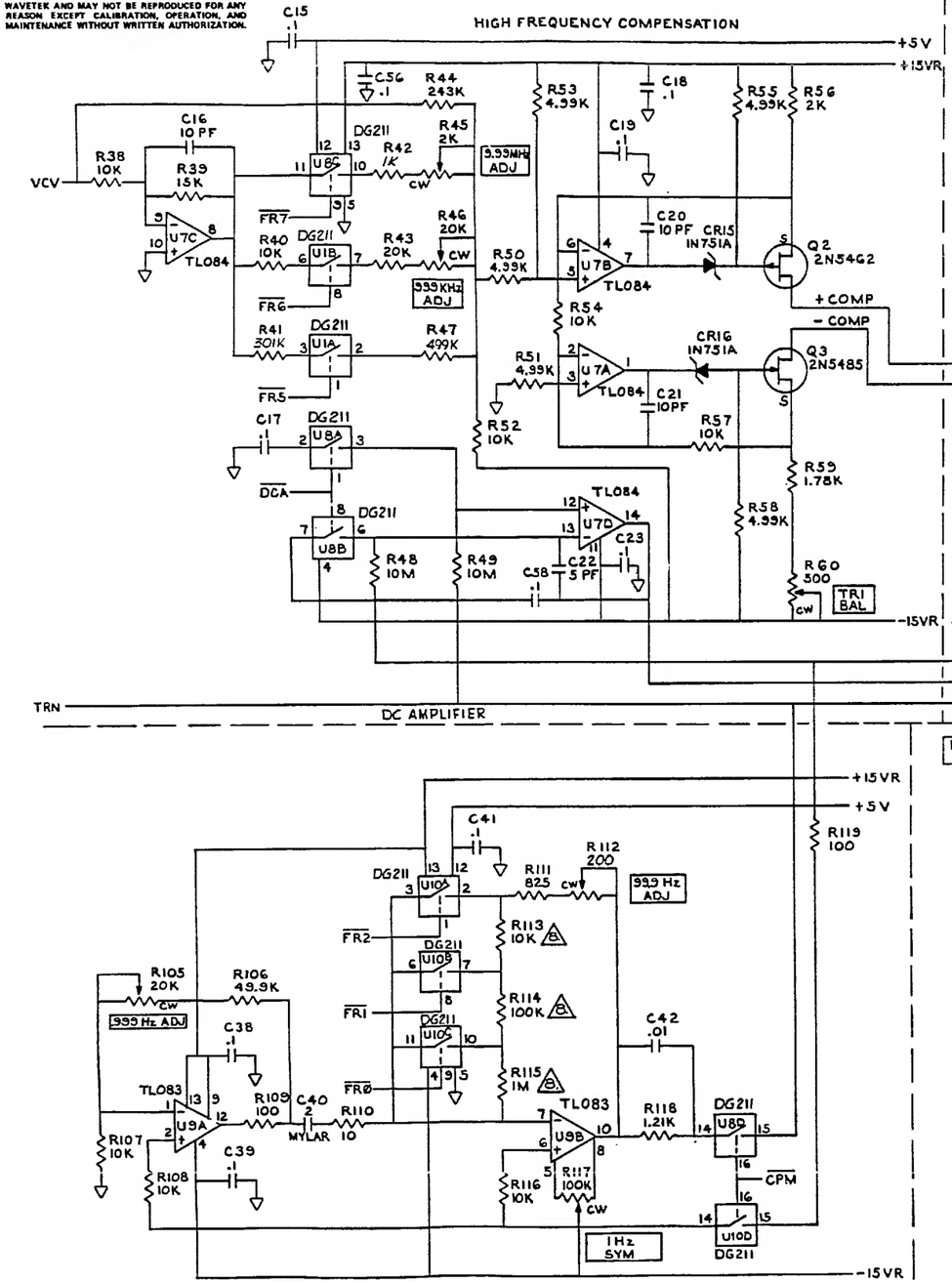
TRIGGER CIRCUIT

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S. THOMPSON 11-23-83
PROJ ENGR PBL 7/15/83
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO, CALIFORNIA
TITLE SCHEMATIC FUNCTION GENERATOR BOARD (A7)
MODEL NO. 270,271, 273,278
DWG NO. 0103-00-0920 REV E
CODE IDENT 23338
SHEET 1 OF 4

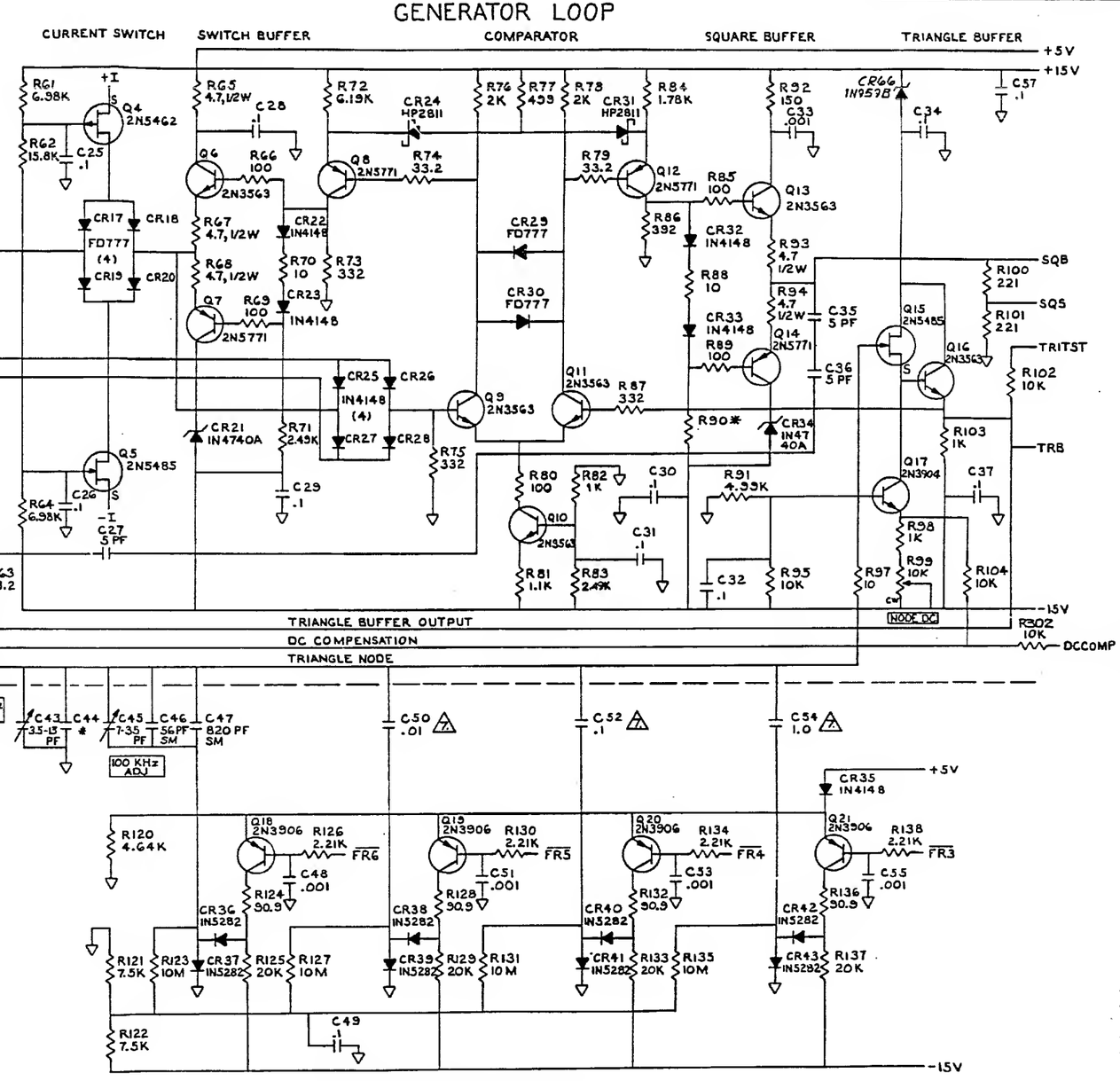
REV	ECN	BY	DATE	APP

FREQUENCY COMPENSATION

HIGH FREQUENCY COMPENSATION



GENERATOR LOOP



TRN — DC AMPLIFIER

CAPACITANCE MULTIPLIER

FREQUENCY RANGE SWITCHES

SEE PAGE 1 (B)

SEE PAGE 1 (7)

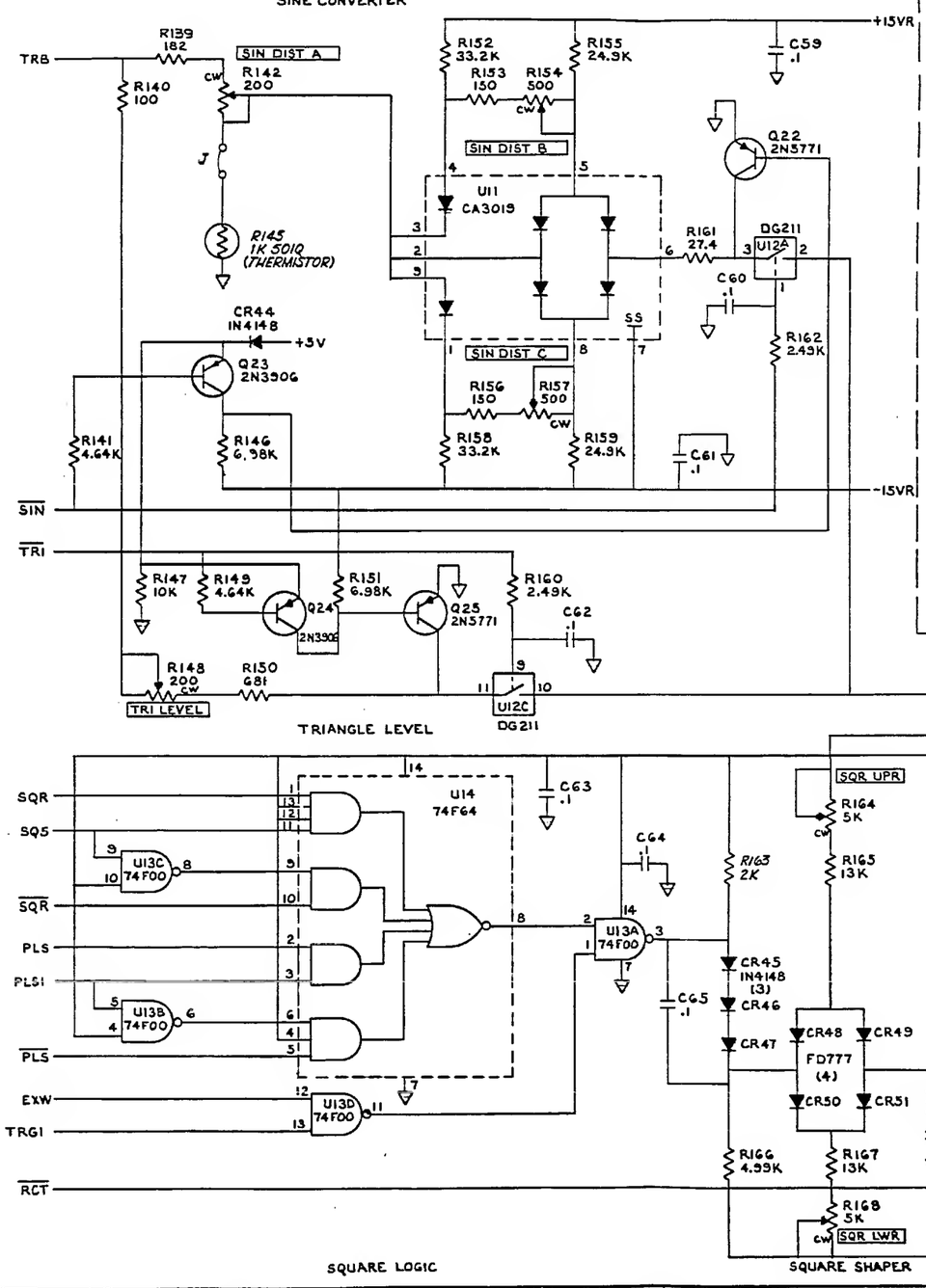
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.THOMPSON	DATE 11-23-81	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR	12/5/81	TITLE: SCHEMATIC FUNCTION GENERATOR BOARD (A7)
FINISH WAVETEK PROCESS	RELEASE APPROVAL		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		MODEL NO. 270, 271, 273, 278
	DO NOT SCALE DWG		DWG NO. 0103-00-0920 REV E
	SCALE		CODE IDENT 23338 SHEET 2 OF 4

REV	ECN	BY	DATE	APP

FUNCTION SELECT

SINE CONVERTER



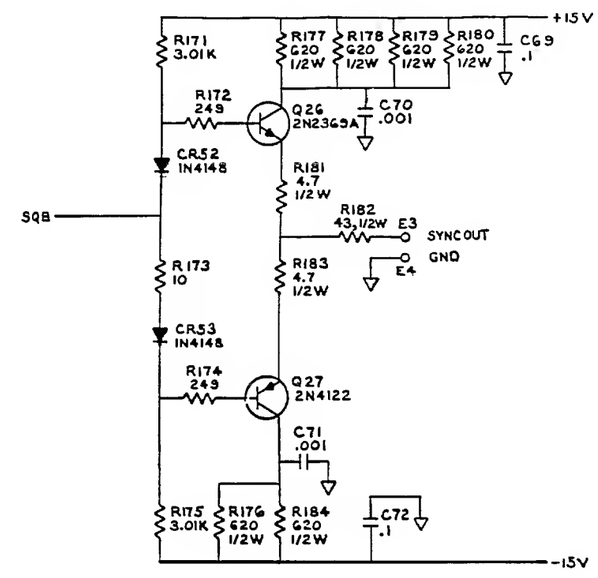
J9 LOGIC

FRQ	1	FRQ
AMP	2	AMP
OST	3	OST
TRL	4	TRL
ANLØ	5	$\overline{FRØ}$
ANL1	6	$\overline{FR1}$
ANL2	7	$\overline{FR2}$
ANL3	8	$\overline{FR3}$
ANL4	9	$\overline{FR4}$
ANL5	10	$\overline{FR5}$
ANL6	11	$\overline{FR6}$
ANL7	12	$\overline{FR7}$
ANL8	13	OAØ
ANL9	14	
ANL10	15	OA2
ANL11	16	MCØ
ANL12	17	MC1
ANL13	18	$\overline{DCA}$
ANL14	19	$\overline{OVR}$
ANL15	20	$\overline{CPM}$
ANL16	21	-TR
ANL17	22	+TR
ANL18	23	EXW
ANL19	24	$\overline{SQR}$
ANL20	25	SQR
ANL21	26	$\overline{SIN}$
ANL22	27	$\overline{TRI}$
ANL23	28	$\overline{RCT}$
ANL24	29	$\overline{PLS}$
ANL25	30	PLS
ANL26	31	
ANL27	32	
PORTIØ	33	OAP
PORTI1	34	FUB

J14 AUX

GND	1	
VCGI	2	VCGI
GND	3	
VCGO	4	VCGO
GND	5	
GND	6	
TRGI	7	TRGI
GND	8	
TRGO	9	TRGO
GND	10	
PLSI	11	PLSI
GND	12	
SQS	13	SQS
GND	14	

SYNC DRIVER



J23 TEST

PATEST	1	PATEST
+15V	R185 2	+15VT
-15V	R186 3	-15VT
	R187 100(3) 4	GND
+5V	5	+5VT
	6	GND
TRITST	7	TRITST
	8	GND
DCCOMP	9	DCCOMP
	10	GND
VCGTST	11	VCGTST
	12	GND
AMPLDC	13	AMPLDC
	14	GND

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.THOMPSON	DATE 11-23-84	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR R86	12/5/84	TITLE SCHEMATIC FUNCTION GENERATOR BOARD (A7)
FINISH WAVETEK PROCESS	RELEASE APPR		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		MODEL NO. 270, 271, 273, 278
	DO NOT SCALE DWG		DWG NO. 0103-00-0920 REV E
	SCALE		CODE IDENT 23338 SHEET 3 OF 4

REV	ECN	BY	DATE	APP

PREAMPLIFIER

OUTPUT AMPLIFIER

J10 POWER: GND (1), GND (2), +5V (3), GND (4), -15V (5), -15V (6), GND (7), GND (8), +15V (9), +15V (10) → +5V, -15V, -15VR, +15V

C123 22/15

U15B CA3083 · U15C CA3083 · U15D CA3083 · U15A CA3083 · CR54 IN751A

Q28 2N5771 · Q29 2N5771

R188 10K · R189 750, .1% · R190 5.76K · R191 1K · R192 750, .1% · R193 10K · R194 750, .1% · R195 2.49K · R196 5.76K · R197 1K · R198 750, .1% · R199 750

C73 .1 · C74 .1 · C75 .1 · C76 .1 · C77 .1 · C78 .1 · C79 .1 · C80 2.7pF · C81 2.7pF · C82 1.5PF · C83 .1

R996 200

U16A CA3096 · U16B CA3096 · OFFSET ADJ

R200 150 · R201 1K · R202 1K · R203 221 · R204 10K · R205 42.2 · R206 3.32K · R207 150 · R208 100 · R209 464 · C86 150 PF · C87 .001 · C88 .1

PATEST

Q30 2N3563 · Q31 2N5771 · Q32 2N2905A · Q33 2N2219A · Q34 · Q35 2N2219A (2) · Q36 · Q37 2N2905A (2)

R210 150 · R211 100 · R212 2K · R213 24.9K · R214 2K · R215 100 · R216 4.99K · R217 909 · R218 51.1 · R219 10 · R220 100 · R221 21.5 · R222 100 · R223 90.9 · R224 750 · R225 21.5 · R226 10 · R227 10 · R228 10 · R229 10 · R230 10 · R231 10 · R232 10 · R233 10

C84 .1 · C85 .1 · C89 .1 · C90 .1 · C91 .1 · C92 .1 · C93 .1 · C94 10PF · C95 .1 · C96 .1 · C97 7-35PF · C98 · C99 .1 · C100 22/15 · C101 .1 · C102 22/15 · C103 .1 · C122 3.5-13

O.A. ROLLOFF · O.A. PEAKING

CR55 IN4148 · CR56 IN4148 · CR57 IN5282 · CR58 IN5282

2800-11-0012 HEAT SINKS (4)

2800-11-0008 HEAT SINK (2)

+15V · -15V

OST

MODEL 275 ONLY

E15 ARB IN · E16 GND · R300 TRIM

R234 10K · R235 4.99K · R236 4.99K · C104 .1 · R239 27.4K · U17C TL084 · R237 2K · R238 1.62K · -15VR · OFFSET ZERO · OFFSET

+15VR · -15VR

XY1 · MULT DC BAL · R241 1K · R243 7.5K · HI AMPL ADJ · R240 4.75K · R242 2K · C105 .1 · C106 .1

LO AMPL ADJ · R251 100K · C107 .1 · MULT. DIST. · R254 499K · R256 1K · R257 1K · R258 4.99K · C108 .1 · U17D TL084 · U17A TL084 · AMPLDC · R264 10K

U18 CA3054 · U19 CA3054 · R244 100 · R245 1.1K · R246 1.1K · R247 100 · R248 1.1K · CR59 IN4148 · CR60 IN823A · R249 1.21K · R250 100 · R252 27.4K · R253 27.4 · R255 20K · R259 27.4 · R260 4.99K · R261 100 · CR61 IN751A · U17B TL084 · C109 22PF · R262 1.21K · R263 2K · CR62 IN4148 · R265 10K · R266 2.49K · R267 7.5K · C110 .1 · C111 .1 · C112 .1 · C113 .1 · -15VR

AMP

XY MULTIPLIER

5. SEE PAGE 1 NOTE: UNLESS OTHERWISE SPECIFIED

XY MULTIPLIER & OFFSET

+5V · R277 4.99K · R278 15K · FUSE SENSE · FU8 · C117 .1 · C118 .1 · U20D LM339 · R285 100K · R286 1M · R287 100K · R288 1M · F1 FUSE P/N 1200-00-0977

R268 CRG3 499K IN4148 · R269 CRG4 499K IN4148 · CRG5 IN4148 · C116 .1 · R270 1M · R271 78.7K · R272 78.7K · R273 1M · R274 78.7K · R275 78.7K · R276 1M · C114 10PF · C115 10PF · OVERVOLTAGE SENSE

U20A LM339 · U20B LM339 · U20C LM339 · OAP · OAØ · OA2

R279 4.99K · R280 2.21K · R281 4.99K · R282 3.01K · R283 4.99K · R284 3.01K · Q38 2N3638A · Q39 2N3904 · Q40 2N3904 · Q41 2N3904 · C119 .1 · C120 .1 · C121 .1

K1 · K2 · K3 · RA31571051 (3) · OUTPUT ATTENUATOR

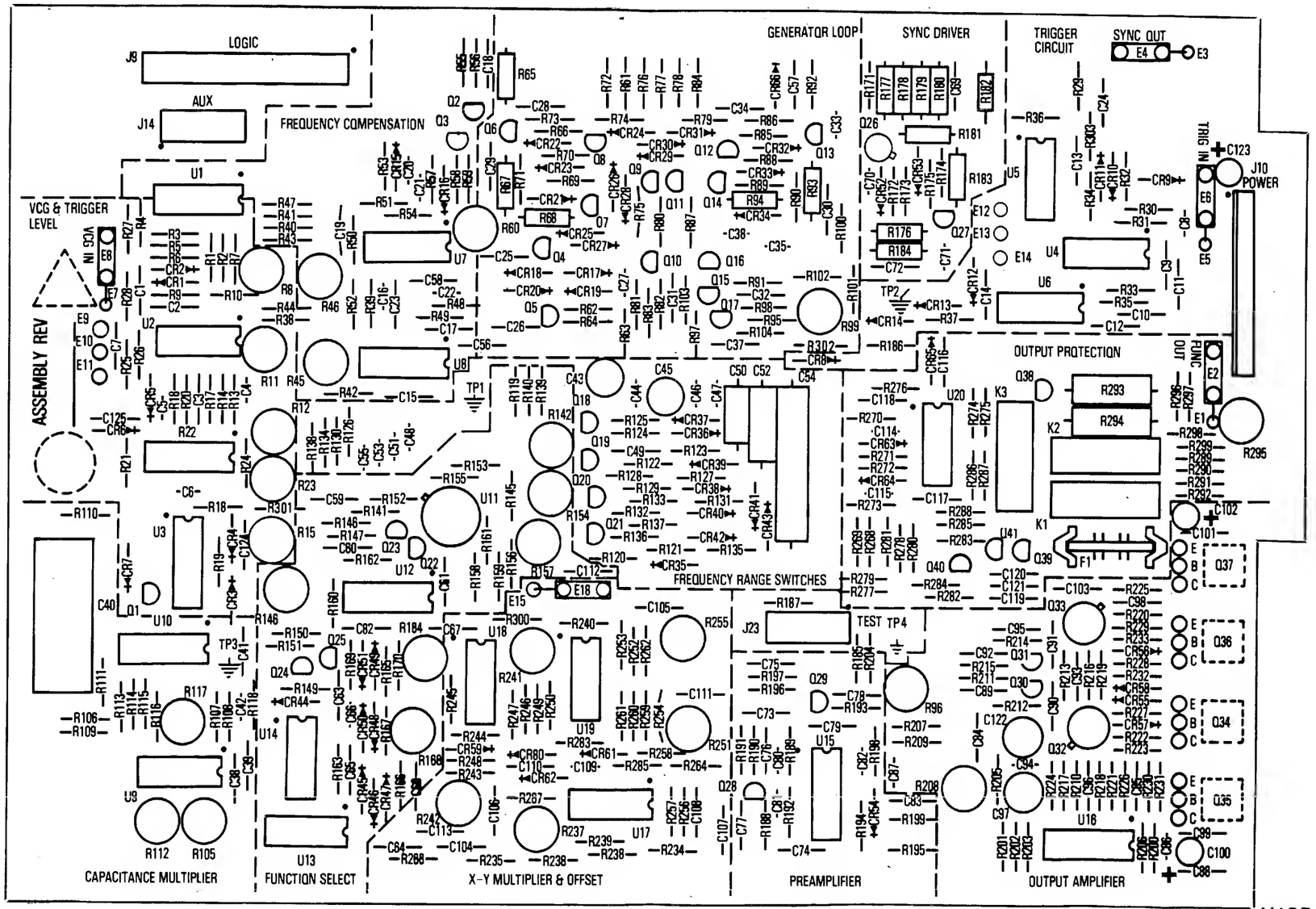
R289 1.96K(4) · R290 · R291 · R292 · R295 20 · ATTEN ADJ · R298 1M · R293 100, 1W · R294 100, 1W · R296 10 · R297 12.4 · R299 1M

E1 FUNC OUT · E2 GND

OUTPUT PROTECTION

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. THOMPSON	DATE 11-23-81	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR RBG		TITLE SCHEMATIC FUNCTION GENERATOR BOARD (A7)
FINISH WAVETEK PROCESS	RELEASE APPROVAL BCA		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 270, 271, 273, 278	DWG NO. 0103-00-0920 REV E
	SCALE	CODE IDENT 23338	SHEET 4 OF 4

BISHOP GRAPHICS/ACCURPRESS REORDER NO. A-2004



MADE FROM 0100-00-0920-3F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: FUNCTION GENERATOR ASSEMBLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO: 278 / DWG NO: 1100-00-0920 / REV
	SCALE		CODE IDENT: 23338 / SHEET 1 OF 1

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, FUNCTION GENERATOR	0101-00-0920	WVTK	0101-00-0920	1
NONE	SCHEMATIC, FUNCTION GENERATOR	0103-00-0920	WVTK	0103-00-0920	1
F1	PCA, OUTPUT FUSE BO	1200-00-0977	WVTK	1200-00-0977	1
NONE	ASSY, XSISTOR MNTG ANGLE	270-1009	WVTK	1206-00-1009	1
C22 C27 C35 C36	CAP, CER, 5PF, 1KV	00-050	CRL	1500-00-5011	4
C114 C115 C16 C20 C21 C8 C94	CAP, CER, 10PF, 1KV	00-100	CRL	1500-01-0011	7
C4 C5	CAP, CER, 100PF, 1KV	00-101	CRL	1500-01-0111	2
C33 C48 C51 C53 C55 C70 C71 C87	CAP, CER, .01MFD, 1KV	DD-102	CRL	1500-01-0211	8
C42	CAP CER MON .01MF 50V, AXIAL	CAC02Z5U103Z100A	CORNG	1500-01-0310	1
C1 C10 C101 C103 C104 C105 C106 C107 C108 C11 C110 C111 C112 C113 C116 C117 C118 C119 C12 C120 C121 C124 C125 C13 C14 C15 C17 C18 C19 C2 C23 C24 C25 C26 C28 C29 C3 C30 C31 C32 C34 C37 C38 C39 C41 C49 C56 C57 C58 C59 C60 C61 C62 C63 C64	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	82

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — REV J — PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C65 C67 C68 C69 C7 C72 C73 C74 C75 C76 C77 C78 C79 C83 C84 C85 C88 C89 C9 C90 C91 C92 C93 C95 C96 C98 C99					
C86	CAP, CER, 150PF, 1KV	00-151	CRL	1500-01-5111	1
C126 C127 C82	CAP, CER, 1.5PF, 1KV	NC01.5PF1KVK750-CR	N1C	1500-01-5507	3
C109 C66 C66T	CAP, CER, 22PF, 1KV	DO-220	CRL	1500-02-2011	3
C6	CAP, CER, 220PF, 1KV	OD-221	CRL	1500-02-2111	1
C80 C81	CAP CER MON 2.7PF 50V	IMCAC2R70	ARCO	1500-02-7505	2
C66T	CAP, MICA, 36PF, 500V	DM15-360J	ARCO	1500-13-6000	1
C46	CAP, MICA, 56PF, 500V	DM15-560J	ARCD	1500-15-6000	1
C47	CAP, MICA, 820PF, 300V	DM15-821F	ARCO	1500-18-2101	1
C40	CAP, MYLR, 2MF, 200V	2MFW205K	AMRAD	1500-42-0504	1
C122 C43	CAP, VAR, 3.5-13PF, 250V	7S-TRIKO-02 3.5/13PF	TRIKO	1500-51-3000	2
C45 C97	CAP, VAR, 7-35PF 250V	7S-TRIKO-02 7/35 PF	TRIKO	1500-53-5000	2
C100 C102 C123	CAP, TANT, 22MF, 15V	1960226X9015KA1	SPRAG	1500-72-2601	3
C50 C52 C54	CAP SET, POLYC MIXED MATCHED SET	180-501	WVTK	1509-80-0008	1

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — REV J — PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	FUNCTION GENERATOR	270-0920	WVTK	1700-00-0920	1
J10	CONN, HEADER	09-60-1101	MOLEX	2100-02-0088	1
J14	CONN, HOUSING, 14 PIN WITH POLARIZING TABS	2100-02-0136	WVTK	2100-02-0136	1
J9	CONN, HOUSING, 34 PIN WITH POLARIZING TABS	2100-02-0138	WVTK	2100-02-0138	1
NONE	TERM	200081	USECO	2100-05-0009	12
TP1 TP2 TP3 TP4	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	4
J23	CONN, HEADER, 14 PIN 2X7	CA-D14RSP100-230-090	CA	2100-05-0053	1
NONE	SPACER, HINGED .750H, .250D6-32 THD	LT3021	LYNTR	2800-03-0009	2
NONE	SPACER .750H, .250 HEX6-32 THRU	2323	SMITH	2800-03-0010	2
NONE	SPACER, SWAGE .562H, .250 01A	BR6310B-0.562-31	LYNTR	2800-04-0017	3
NONE	HEAT SINK	207	WAKE	2800-11-0001	2
NONE	TRANSIPAD	10160	METRS	2800-11-0004	2
NONE	JUMPER	461-2871-01-03-10	CAMBN	3000-00-0034	2
E10 E11 E12 E13 E14 E9	PINS, JUMPER	450-3704-01-03	CAMBN	3000-00-0035	6

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — REV J — PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	DIGI-CLIP	MC-20	CMPCP	3000-00-0093	4
NONE	DIGI-GUIDE	MC-10-1/2	CMPCP	3000-00-0094	2
K1 K2 K3	RELAY, REED, FORM-A	1503-1D-2	WABSH	4500-00-0007	3
R295	POT, TRIM, 20	91AR20	BECK	4600-02-0000	1
R11 R117 R12 R15 R251	POT, TOP TRIM, 20T, 100K	68WR100K	BECK	4609-90-0001	5
R99	POT, TOP TRIM, 20T, 10K	68WR10K	BECK	4609-90-0002	1
R105 R255 R46	POT, TOP TRIM, 20T, 20K	68WR20K	BECK	4609-90-0003	3
R237 R242 R45	POT, TOP TRIM, 20T, 2K	68WR2K	BECK	4609-90-0004	3
R241 R8	POT, TOP TRIM, 20T, 1K	68WR1K	BECK	4609-90-0005	2
R164 R168	POT, TOP TRIM, 20T, 5K	68WR5K	BECK	4609-90-0013	2
R208 R23	POT, TOP TRIM, 20T, 100	68WR100	BECK	4609-90-0019	2
R112 R142 R148 R96	POT, TOP TRIM, 20T, 200	68WR200	BECK	4609-90-0020	4
R154 R157 R60	POT, 20T, TOP TRIM, 500 OHM	68WR500	BECK	4609-90-0023	3
R182	RES, C, 1/2W, 5%, 43	RCR20G430JS	AB	4700-25-0430	1
R181 R183 R65 R67 R68 R93 R94	RES, C, 1/2W, 5%, 4.7	RC-1/2-4R7J	STKPL	4700-25-0479	7

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — REV J — PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R176 R177 R178 R179 R180 R184	RES, C, 1/2W, 5%, 620	RC-1/2-621J	STKPL	4700-25-6200	6
R189 R192 R194 R198	RES, MF, 1/8W, .1%, 750	RN55E-7500B	MEPCO	4701-02-7500	4
R109 R119 R140 R169 R185 R186 R187 R211 R215 R220 R222 R244 R247 R250 R261 R66 R69 R80 R85 R89	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	20
R103 R14 R17 R18 R191 R197 R20 R201 R202 R256 R257 R42 R82 R98	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	14
R102 R104 R107 R108 R116 R147 R188 R193 R204 R234 R264 R265 R301 R302 R38 R40 R52 R54 R57 R6 R95	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	21
R285 R287 R33 R35	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	4
R10 R16 R270 R273 R276 R286 R288 R298 R299 R3	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	10
R110 R173 R219 R226 R227 R228 R229 R230 R231 R232 R233 R296 R70 R88 R97	RES, MF, 1/8W, 1%, 10	RN55D10R0F	MEPCD	4701-03-1009	15
R245 R246 R248 R81	RES, MF, 1/8W, 1%, 1.1K	RN55D-1101F	TRW	4701-03-1101	4
R118 R249 R262	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	3
R297	RES, MF, 1/8W, 1%, 12.4	RN55D-12R4F	TRW	4701-03-1249	1

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — REV J — PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R165 R167	RES, MF, 1/8W, 1%, 13K	RN55D-1302F	TRW	4701-03-1302	2
R153 R156 R200 R207 R210 R92	RES, MF, 1/8W, 1%, 150	RN55D-1500F	TRW	4701-03-1500	6
R278 R39	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	2
R1 R2	RES, MF, 1/8W, 1%, 150K	RN55D-1503F	TRW	4701-03-1503	2
R62	RES, MF, 1/8W, 1%, 15.8K	RN55D-1582F	TRW	4701-03-1582	1
R238	RES, MF, 1/8W, 1%, 1.62K	RN55D-1621F	TRW	4701-03-1621	1
R59 R84	RES, MF, 1/8W, 1%, 1.78K	RN55D-1781F	TRW	4701-03-1781	2
R139	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	1
R289 R290 R291 R292	RES, MF, 1/8W, 1%, 1.96K	RN55D-1961F	TRW	4701-03-1961	4
R163 R212 R214 R263 R56 R75 R78	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	7
R125 R129 R133 R137 R26 R304 R305 R43	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	8
R221 R225	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	2
R100 R101 R203	RES, MF, 1/8W, 1%, 221	RN55D-2210F	TRW	4701-03-2210	3
R126 R130 R134 R138 R280	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	5
R24	RES, MF, 1/8W, 1%, 23.7K	RN55D-2372F	TRW	4701-03-2372	1

WAVETEK PARTS LIST — TITLE: PCA, FUNCTION GEN — ASSEMBLY NO. 1100-00-0920 — REV J — PAGE 6

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, FUNCTION GEN
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 278 — DWG NO 1100-00-0920 — REV J
	SCALE		CODE IDENT 23338 — SHEET 1 OF 2

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R44	RES, MF, 1/8W, 1%, 243K	RN55D-2433F	TRW	4701-03-2433	1
R172 R174	RES, MF, 1/8W, 1%, 249	RN550-2490F	TRW	4701-03-2490	2
R160 R162 R170 R195 R266 R303 R32 R34 R36 R71 R83 R9	RES, MF, 1/8W, 1%, 2.49K	RN550-2491F	TRW	4701-03-2491	12
R155 R159 R213	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	3
R239 R252	RES, MF, 1/8W, 1%, 27.4K	RN55D-2742F	TRW	4701-03-2742	2
R161 R253 R259	RES, MF, 1/8W, 1%, 27.4	RN55D-27R4F	TRW	4701-03-2749	3
R171 R175 R282 R284	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	4
R25	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	1
R41	RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	1
R73 R75 R87	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	3
R206 R30	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	2
R152 R158	RES, MF, 1/8W, 1%, 33.2K	RN55D-3322F	TRW	4701-03-3322	2
R63 R74 R79	RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	3
R7	RES, MF, 1/8W, 1%, 3.57K	RN55D-3571F	TRW	4701-03-3571	1
R86	RES, MF, 1/8W, 1%, 392	RN550-3920F	TRW	4701-03-3920	1
R205	RES, MF, 1/8W, 1%, 42.2	RN550-42R2F	TRW	4701-03-4229	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN | ASSEMBLY NO. 1100-00-0920 | REV J

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R209	RES, MF, 1/8W, 1%, 464	RN55D-4640F	TRW	4701-03-4640	1
R120 R141 R149	RES, MF, 1/8W, 1%, 4.64K	RN550-4641F	TRW	4701-03-4641	3
R240	RES, MF, 1/8W, 1%, 4.75K	RN550-4751F	TRW	4701-03-4751	1
R77	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	1
R166 R19 R21 R216 R235 R236 R258 R260 R27 R277 R279 R28 R281 R283 R29 R4 R5 R50 R51 R53 R55 R58 R91	RES, MF, 1/8W, 1%, 4.99K	RN550-4991F	TRW	4701-03-4991	23
R106	RES, MF, 1/8W, 1%, 49.9K	RN550-4992F	TRW	4701-03-4992	1
R13 R254 R268 R269 R47	RES, MF, 1/8W, 1%, 499K	RN55D-4993F	TRW	4701-03-4993	5
R218	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	1
R190 R196 R90T	RES, MF, 1/8W, 1%, 5.76K	RN55D-5761F	TRW	4701-03-5761	3
R72	RES, MF, 1/8W, 1%, 6.19K	RN55D-6191F	TRW	4701-03-6191	1
R150	RES, MF, 1/8W, 1%, 681	RN55D-6810F	TRW	4701-03-6810	1
R146 R151 R61 R64	RES, MF, 1/8W, 1%, 6.98K	RN55D-6981F	TRW	4701-03-6981	4
R199 R224	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	2
R121 R122 R243 R267 R31	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	5
R271 R272 R274 R275	RES, MF, 1/8W, 1%, 78.7K	RN55D-7872F	TRW	4701-03-7872	4

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN | ASSEMBLY NO. 1100-00-0920 | REV J

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R111	RES, MF, 1/8W, 1%, 825	RN55D-8250F	TRW	4701-03-8250	1
R37	RES, MF, 1/8W, 1%, 8.25K	RN55D-8251F	TRW	4701-03-8251	1
R217	RES, MF, 1/8W, 1%, 909	RN55D-9090F	TRW	4701-03-9090	1
R124 R128 R132 R136 R223	RES, MF, 1/8W, 1%, 90.9	RN55D-90R9F	TRW	4701-03-9099	5
R293 R294	RES, MF, 1W, 1%, 100	RN70D-1000F	TRW	4701-33-1000	2
R22	RES NETWORK 1K 2W 16PIN DIP	4116R-001-102	BOURN	4770-00-0019	1
R113 R114 R115	RES, MF, MIXED SET	4789-00-0043	WVTK	4789-00-0043	1
R123 R127 R131 R135 R48 R49	RES, MF, 1/4W, 1%, 10M	CC1005F	AB	4799-00-0056	6
CR11 CR15 CR16 CR54 CR61	DIODE, ZENER, 5.1V, 5% TOL, 500MW, G/B, 1N751A	1N751A	FAIR	4801-01-0751	5
CR60	DIODE, ZENER, 6.2V, 1N823	1N823A	MOT	4801-01-0823	1
CR4 CR6 CR66	DIODE, ZENER 500MW SILICON PLANAR	1N959	SIEM	4801-01-0959	3
CR21 CR34	DIODE, ZENER 10V, GLASS SILICON, 1W	1N4740A	MOT	4801-01-4740	2
CR36 CR37 CR38 CR39 CR40 CR41 CR42 CR43 CR57 CR58	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	10

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN | ASSEMBLY NO. 1100-00-0920 | REV J

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR17 CR18 CR19 CR20 CR29 CR30 CR48 CR49 CR50 CR51	DIODE, ULTRA FAST	F0777	FAIR	4807-02-0777	10
CR1 CR10 CR12 CR13 CR14 CR2 CR22 CR23 CR25 CR26 CR27 CR28 CR3 CR32 CR33 CR35 CR44 CR45 CR46 CR47 CR5 CR52 CR53 CR55 CR56 CR59 CR62 CR63 CR64 CR65 CR9	DIODE 1N4148 COMPUTER, G/P, 75V, 200MA, SWITCHING	1N4148	FAIR	4807-02-6666	31
CR24 CR31	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	2
CR7 CR8	DIODE, M/PR, FD-777 QTY: 2: 4807-02-0777	164-501-93	WVTK	4898-00-0004	1
G33	TRANS 2N2219A NPN GENERAL PURPOSE TO-5	2N2219A	NSC	4901-02-2191	1
G26	TRANS, SILICON PLANAR, EPITAXIAL NPN	2N2369A	MOT	4901-02-3691	1
G32	TRANS 2N2905A PNP GENERAL PURPOSE TO-5	2N2905A	NSC	4901-02-9051	1
G10 G11 G13 G16 G30 G6 G9	TRANS, NPN, TO-92	2N3563	FAIR	4901-03-5630	7
G38	TRANS, GENERAL PURPOSE, PNP, TO-92	2N3638A	CARTR	4901-03-6381	1
G1	TRANS, GENERAL PURPOSE, NPN, TO-92	2N3903	NSC	4901-03-9030	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN | ASSEMBLY NO. 1100-00-0920 | REV J

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q17 Q39 Q40 Q41	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	4
Q18 Q19 Q20 Q21 Q23 Q24	TRANS 2N3906 PNP GENERAL PURPOSE TO-92	2N3906	FAIR	4901-03-9060	6
Q27	TRANS, GENERAL PURPOSE, PNP, TO-92	2N4122	NSC	4901-04-1220	1
Q2 Q4	TRANS, P-CHANNEL JFETS	2N5462	MOT	4901-05-4620	2
Q15 Q3 Q5	TRANS, N-CHANNEL JFETS	2N5485	MOT	4901-05-4850	3
Q12 Q14 Q22 Q25 Q28 Q29 Q31 Q7 Q8	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	9
R145	THERMISTER	1K-501-K	MC1	5300-00-0011	1
U9	OP AMP, DUAL JFET INPUT	TL083CN	TI	7000-00-8300	1
U17 U2 U7	OP AMP, QUAD BIMOS MOS/FET INPUT	TL084CN	TI	7000-00-8400	3
U20	COMPARATORS, QUAD VOLTAGE	MLM339P	MOT	7000-03-3900	1
U4	IC	NE529N	SIG	7000-05-2900	1
U11	DIODE, ULTRA FAST, LOW CAPACITANCE	CA-3019	RCA	7000-30-1900	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN | ASSEMBLY NO. 1100-00-0920 | REV J

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U18 U19	TRANS ARRAY, DIFFERENTIAL AMP, DUAL 1N	CA-3054	RCA	7000-30-5400	2
U15	TRANS ARRAY, GENERAL PURPOSE, NPN	CA3083	FAIR	7000-30-8300	1
U16 U3	TRANS ARRAY, NPN/PNP	CA-3096AE	RCA	7000-30-9600	2
U1 U10 U12 U8	SW, QUAD ANALOG, CMOS	DG211CJ	SILCON	8000-02-1100	4
U13 U5	GATE, NAND, QUAD 2INP, TTL	74F00PC	FAIR	8000-74-0002	2
U14	4-2-3-2 INP AOI, TTL	74F64PC	FAIR	8000-74-6402	1
U6	FLIP-FLOP DUAL, D-POS EDGE TRIG, TTL	74F74PC	FAIR	8000-74-7402	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN | ASSEMBLY NO. 1100-00-0920 | REV J

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, FUNCTION GEN
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 278 | DWG NO 1100-00-0920 | REV J
	SCALE		CODE IDENT 23338 | SHEET 2 OF 2

REV	ECN	BY	DATE	APP
A	ECN 4777	IRO	5-84	
B	ECO # 84-010	NGS	1-24-89	TPMB

MICROPROCESSOR/MEMORY

TEST J8

E, ADR15, ADR14, AS, ADR13, ADR12, NMI, ADR11, ADR10, ADR9, ADR8, AD7, AD6, AD5, TEST, AD4, AD3, +5V, AD2, N.C., AD1, N.C., AD0, R/W

MICROPROCESSOR

U1A, U1B: 1/2 74LS00; U2: 14040; R8: 10K SIP; C5: .1/50V; CR3: IN4148; DS1: BEEPER QMB-06; R2: 2.49K; Q1: 2N3904; C4: .1/50V; C3: 27pF; Y1: 4MHz; C2: 27pF; C1: .001; CR1, CR2: 2811(2); R1: 10K SIP

PORT21, PORT22, PORT20, N/C, N/C → P21, P22, P20, P23, P24

U3: 6803

1M(4); R3, R4, R5, R6

PORT10, PORT11, PORT12, PORT13, PORT14, PORT15, PORT16, PORT17 → P10, P11, P12, P13, P14, P15, P16, P17

P40 ADR8, P41 ADR9, P42 ADR10, P43 ADR11, P44 ADR12, P45 ADR13, P46 ADR14, P47 ADR15

NMI, IRQ

ADDRESS LATCH

R1: 10K SIP; R8: 10K SIP; C6: .1/50V; R7: 2.2K SIP

R/W, AS, P30 AD0, P31 AD1, P32 AD2, P33 AD3, P34 AD4, P35 AD5, P36 AD6, P37 AD7

U4: 74LS373 — D0–D7 / Q0–Q7 → ADR0–ADR7

GPIB ADDRESS

R1: 10K SIP; R8: 10K SIP; C7: .1/50V; SW1

GA0, GA1, GA2, GA3, GA4, FPADEN, ETR

U5: 74LS240 — I1–I8 / Ø1–Ø8 → AD0–AD7

R32: 2.2K SIP; R7: 2.2K SIP

DATA LATCH

R32: 2.2K SIP; C47: .1/50V

U25: 74LS373 — AD0–AD7 → DATA0–DATA7

ROM

U9, U10: ROM1, ROM2; ADR12, ADR0–ADR11; AD0–AD7; C16, C17: .1/50V

RAM

U11, U12: 6116L; RAM1, RAM2; R11: 2.21K; R12: 2.21K; C18, C19: .1/50V

RAM PWR (2A2)

WRITE PULSE

C15: .1/50V; U1D: 1/2 74LS00; U1C; R/W, E → WRP

GPIB INTERFACE

IEEE-488 INTERFACE

U6: 68488 — RESET, T/R, CLK, D0–D7, CS, R/W, RS0, RS1, RS2, ASE, IRQ, DMA

C8: .1/50V

ALTERNATE BUS DRIVERS

U7A: 75160A; U8A: 75161A; C9: .1/50V; C10, C11: .1/50V; C12: .1/50V; R9: 100; R10: 1DO

IEEE-488 CONN J2

IB0 DIO1, IB1 DIO2, IB2 DIO3, IB3 DIO4, IB4 DIO5, IB5 DIO6, IB6 DIO7, IB7 DIO8

REN, IFC, DAC, RFD, DAV, EOI, ATN, SRQ

PORT20

IEE488 BUS DRIVERS

U7B: 3447; U8B: 3447; C13: .1/50V; C14: .1/50V

IEEE-488 CONN J2

U6-28, U6-25, U6-16, U6-36, U6-34, U6-32, U6-30, U6-17, U8A-18, U6-27, U6-23, U6-35, U6-33, U6-31, U6-29, U6-26, U8A-19

18,19,20,21,22,23,24

ADDRESS DECODER

U13; R55: 10K; R13: 2.2K SIP

P/N 8600-00-0237

I0 KYBD, I1 DISP, I2 GPIB, I3 RAM2, I4 ROM1, I5 ROM2, I6 RAM1, I7 ANALOG

POWER

CR4: MBR120; CR5: 2811; BT1

NOTES

6. PROM'S PROGRAMMED PER MODEL, SEE PARTS LIST.
5. LAST REFERENCE DESIGNATORS USED ARE: R61, C72, CR19, VR4, SW1, U29, Q2, BT1
4. ALL CAPACITORS ARE SHOWN IN MICRO-FARADS.
3. ALL RESISTORS ARE SHOWN IN OHMS.
2. ALL DIODES ARE FD6666.
1. REFERENCE DESIGNATORS SHOWN ARE PARTIAL, PREFIX WITH ASSEMBLY REF DES (A6).

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS

DRAWN S.CHERMACK 1-8-83 | PROJ ENGR | RELEASE APPROV | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030 | DO NOT SCALE DWG | SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: SCHEMATIC MICRO PROC/POWER SUPPLY BOARD (A6)

MODEL NO 270 SERIES | DWG NO. 0103-00-2202 | REV B | CODE IDENT 23338 | SHEET 1 OF 3

SAMPLE AND HOLD

ANALOG DECODER

DAC

SAMPLE AND HOLD

BATTERY TEST AND RESET

DISPLAY

AUX BUFFERS

ANALOG REGISTERS

ANALOG INTERFACE

AUX

NOTE: UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.CHERMACK	DATE 1/8/83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/8/83	TITLE SCHEMATIC MICRO PROC/POWER SUPPLY BOARD (A6)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°		
	DO NOT SCALE DWG		MODEL NO. 270 SERIES
	SCALE		DWG NO. 0103-00-2202 REV B
			CODE IDENT 23338 SHEET 2 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

POWER SUPPLY

REV	ECN	BY	DATE	APP

TRANSFORMER J1

45 VAC 1
45 VAC 2
15 VAC 3
15 VAC 4
GND 5
N/C 6 ← N/C
N/C 7 ← N/C
N/C 8 ← N/C
5 VAC 9
5 VAC 10

CR7 3N254

CR8 IN4002
VR1 LM317
R33 1.8, ½W, CARB
R34 3.92K
C70 100/25V
R35 499
CR9
R36 3.92 K
C69 .1/50V
U26A ½ TL082
R37 1.21K
R38 2.74K
R39 500
R40 1.78K
CR10 IN823A
R41 10K
C48 4700/25V
C49 .1/50V
C52 .1/50V
C53 1000/16V

CR11
R42 3.92K
U26B ½ TL082
R46 4.99K
R47 200
R48 10K
C50 4700/25V
C51 .1/50V
C54 .1/50V
C55 1000/16V
VR2 LM337
R43 3.92K
C68 100/25V
R44 499
R45 1.8, ½W, CARB
CR12 IN4002(2)

-22V → J9 1, 2 FAN, 3

CR13 MDA970A2
CR14
VR3 LM317
R50 1.1K
R53 1K
C56 6800/16V
C57 .1/50V
R49 3.16 K
C58 .1/50V
C59 1000/16V

CR16 IN4002
VR4 LM317
R52 301
R54 49.9K
CR15 3N254
C60 470/50V
C61 .1/50V
R51 10K
C62 .1/50V
C63 470/50V

+45V J7-1 (2A8)

+5V TEST JUMPER E2 E1

+15V
+15V
-15V
-15V
+5V
+5V

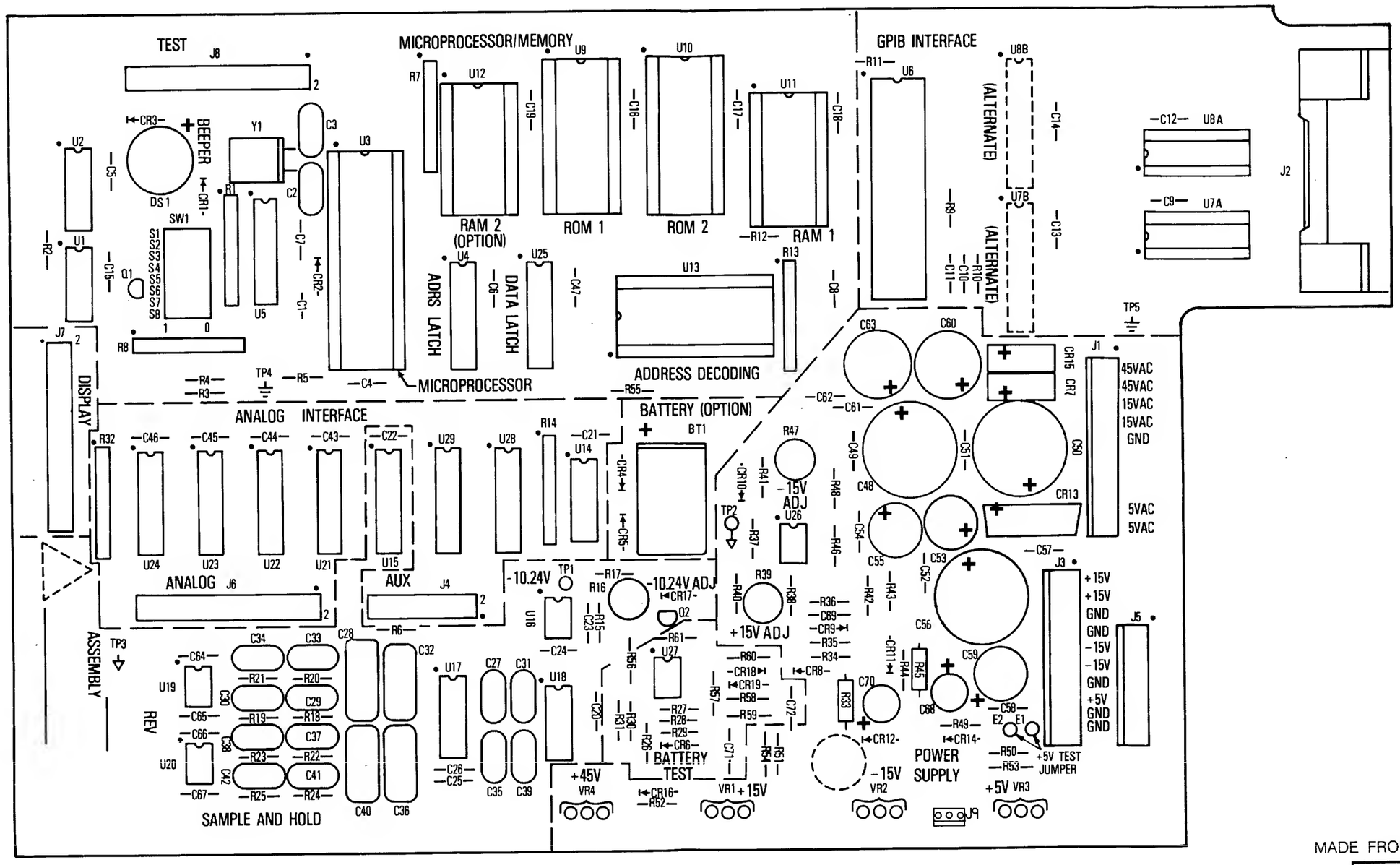
ANALOG POWER J5
1 +15V
2 +15V
3
4
5
6
7
8 -15V
9 -15V
10

AUX POWER J3
1 +5V
2
3
4
5
6
7
8
9
10

TP2 TP3 TP4 TP5

NOTE. UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.CHERMACK	DATE 1-8-83	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR R.B.	2/15/83	TITLE SCHEMATIC MICRO PROC/POWER SUPPLY BOARD (A6)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°		
	DO NOT SCALE DWG	MODEL NO. 270 SERIES	DWG NO. 0103-00-2202 REV B
	SCALE	CODE IDENT 23338	SHEET 3 OF 3



MADE FROM 0100-00-2202-3B

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: MICRO PROC/POWER SUPPLY

MODEL NO	ASSY. NO	REV
278	1100-00-2202	
CODE IDENT 23338	SHEET 1 OF 1	

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, MICRO-PRDC/GPIB BOARD	0101-00-2202	WVTK	0101-00-2202	1
NONE	SCHEMATIC MICRO-PRDC/GPIB BOARD	0103-00-2202	WVTK	0103-00-2202	1
C1	CAP,CER,.001MF,1KV	DD-102 LONG LEAD	CRL	1500-01-0201	1
C10 C11 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C4 C43 C44 C45 C46 C47 C49 C5 C51 C52 C54 C57 C58 C6 C61 C62 C64 C65 C66 C67 C69 C7 C71 C72 C8	CAP,CER,MCN,.1MF,50V, AXIAL	CAC03Z5U104Z050A	CDRNC	1500-01-0405	41
C27 C31 C35 C39	CAP,CER,22PF,1KV	DD-220	CRL	1500-02-2011	4
C2 C3	CAP,MICA,27PF,500V	DM15-270J	ARCD	1500-12-7000	2
C29 C30 C33 C34 C37 C38 C41 C42	CAP,910PF,100V,5%	DM15-911J	ARCD	1500-19-1100	8
C68 C70	CAP,ELECT,100MF,35V RADIAL LEAD,SP .20	ULB1V101M	NICH	1500-31-0102	2
C53 C55 C59	CAP,ELECT,1000MF/16V RADIAL LEAD, SP .20	NRE102M16V10X20	NIC	1500-31-0211	3
C60 C63	CAP,ELECT,470MF/50V RADIAL LEAD, SP .30	CRE SERIES 470/50	CAPAR	1500-34-7103	2
C48 C50	CAP,ELECT,4700MF/25V RADIAL LEAD, SP .50	NRE 4700/25	NIC	1500-34-7202	2

WAVETEK PARTS LIST	TITLE: ASSY MICRO-PRDC/GPIB BOARD	ASSEMBLY NO.: 1100-00-2202	REV: C
		PAGE 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C56	CAP,ELECT,6800MF,16V RADIAL LEAD, SP .50	NRE 6800/16	NIC	1500-36-8201	1
C32 C36 C40	CAP,MYLAR,.1MF,100V	225P10491W03	SPRAG	1500-41-0444	3
C28	CAP,MYLAR,1MF,100V,RADIAL	PMT2R1 0K100	ITT	1500-41-0524	1
NONE	DRILL DRWG, MICRO-PRDC/GPIB BOARD	270-2202	WVTK	1700-00-2202	1
J1 J3	CONN, HEADER	09-60-1101	MOLEX	2100-02-0088	2
J5	CONN,HEADER, 10 PIN	1-640456-0	AMP	2100-02-0133	1
J4	CONN,HOUSING,20 PIN WITH POLARIZING TABS	2100-02-0137	WVTK	2100-02-0137	1
J6 J7	CONN,HOUSING,34 PIN WITH POLARIZING TABS	2100-02-0138	WVTK	2100-02-0138	2
NONE	SKT,IC,16PIN	DILB16P-108T	BURND	2100-03-0028	2
NONE	SKT,IC,24PIN	DILB-24P-108	BURND	2100-03-0029	2
U6A	SKT,IC,40PIN	DILB40P-108T	BURND	2100-03-0030	1
NONE	SKT,IC,28PIN	DILB28P-108T	BURND	2100-03-0055	3
NONE	SOCKET,8 PIN	DILB08P-108T	BURND	2100-03-0063	2
NONE	TERM	2000B1	USECO	2100-05-0009	12

WAVETEK PARTS LIST	TITLE: ASSY MICRO-PRDC/GPIB BDARD	ASSEMBLY NO.: 1100-00-2202	REV: C
		PAGE 2	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
TP1 TP2 TP3 TP4 TP5	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	5
J8	CONN,HEADER, 34 PIN	929836-01-17	AP	2100-05-0041	1
J2	CONNECTOR,MOD FRDM: 2100-02-0126	2100-99-0062	WVTK	2100-99-0062	1
Y1	CRYSTAL,4MHZ	180-502	MTRON	2300-99-0004	1
	RIVET 1/8X3/16L	1125-0406	AVDEL	2800-12-0011	1
NONE	JUMPER	461-2871-01-03-10	CAMBN	3000-00-0034	1
E1 E2	PINS,JUMPER	450-3704-01-03	CAMBN	3000-00-0035	2
DS1	BEEPER	GMB-06	STMIC	3000-00-0085	1
NONE	BATTERY HOLDER	3000-00-0090	WVTK	3000-00-0090	1
BT1	BATTERY,LITHIUM,3V	BR-1/2A	PANAS	4000-02-0007	1
R16 R47	PDT,TRIM,200	91AR200	BECK	4600-02-0101	2
R39	PDT,TRIM,500	91AR500	BECK	4600-05-0104	1
R33 R45	RES,C,1/2W,5%,1.8	RC-1/2-1R8J	STKPL	4700-25-0189	2
R10 R9	RES,MF,1/8W,1%,100	RN55D-1000F	TRW	4701-03-1000	2
R53	RES,MF,1/8W,1%,1K	RN55D-1001F	TRW	4701-03-1001	1
R15 R30 R41 R48 R51 R55 R60	RES,MF,1/8W,1%,10K	RN55D-1002F	TRW	4701-03-1002	8

WAVETEK PARTS LIST	TITLE: ASSY MICRO-PROC/GPIB BDARD	ASSEMBLY NO.: 1100-00-2202	REV: C
		PAGE 3	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R61					
R27 R3 R4 R5 R57 R58 R6	RES,MF,1/8W,1%,1M	RN55D-1004F	TRW	4701-03-1004	7
R50	RES,MF,1/8W,1%,1.1K	RN55D-1101F	TRW	4701-03-1101	1
R37	RES,MF,1/8W,1%,1.21K	RN55D-1211F	TRW	4701-03-1211	1
R26	RES,MF,1/8W,1%,12.4K	RN55D-1242F	TRW	4701-03-1242	1
R40	RES,MF,1/8W,1%,1.78K	RN55D-1781F	TRW	4701-03-1781	1
R11 R12	RES,MF,1/8W,1%,2.21K	RN55D-2211F	TRW	4701-03-2211	2
R28	RES,MF,1/8W,1%,2.37K	RN55D-2371F	TRW	4701-03-2371	1
R2	RES,MF,1/8W,1%,2.49K	RN55D-2491F	TRW	4701-03-2491	1
R38	RES,MF,1/8W,1%,2.74K	RN55D-2741F	TRW	4701-03-2741	1
R29	RES,MF,1/8W,1%,27.4K	RN55D-2742F	TRW	4701-03-2742	1
R52	RES,MF,1/8W,1%,301	RN55D-3010F	TRW	4701-03-3010	1
R18 R19 R20 R21 R22 R23 R24 R25	RES,MF,1/8W,1%,301K	RN55D-3013F	TRW	4701-03-3013	8
R49	RES,MF,1/8W,1%,3.16K	RN55D-3161F	TRW	4701-03-3161	1
R31	RES,MF,1/8W,1%,3.83K	RN55D-3831F	TRW	4701-03-3831	1
R34 R36 R42 R43	RES,MF,1/8W,1%,3.92K	RN55D-3921F	TRW	4701-03-3921	4

WAVETEK PARTS LIST	TITLE: ASSY MICRO-PROC/GPIB BDARD	ASSEMBLY NO.: 1100-00-2202	REV: C
		PAGE 4	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R35 R44 R59	RES,MF,1/8,1%,499	RN55D-4990F	TRW	4701-03-4990	3
R46	RES,MF,1/8W,1%,4.99K	RN55D-4991F	TRW	4701-03-4991	1
R54	RES,MF,1/8W,1%,49.9K	RN55D-4992F	TRW	4701-03-4992	1
R56	RES,MF,1/8W,1%,6.19K	RN55D-6191F	TRW	4701-03-6191	1
R17	RES,MF,1/8W,1%,6.81K	RN55D-6811F	TRW	4701-03-6811	1
R1 R8	RES NETWORK 10K 2% 10PIN SIP BUSS	4310R-101-103	BOURN	4770-00-0008	2
R13 R14 R32 R7	RES NETWORK 2.2K 2% 10PIN SIP BUSS	4310R-101-222	BOURN	4770-00-0011	4
CR10	DIDDE, ZENER, 6.2V, IN823	IN823A	MOT	4801-01-0823	1
CR12 CR14 CR16 CR8	DIODE,1N4002 GEN PURPOSE RECT. 100V,1A	1N4002	FAIR	4801-02-0001	4
CR15 CR7	DIODE, RECTIFIER, BRIDGE	3N254	MDT	4801-02-0254	2
CR4	DIDDE, RECT, SCH BARRIER	MBR 120	MOT	4806-02-0120	1
CR11 CR17 CR3 CR6 CR9	DIDDE 1N4148 COMPUTER,O/P,75V,200MA,SWITCHING	1N4148	FAIR	4807-02-6666	5
CR1 CR18 CR19 CR2 CR5	DIODE 5082-2811	5082-2811	HP	4809-02-2811	5

WAVETEK PARTS LIST	TITLE: ASSY MICRO-PROC/GPIB BOARD	ASSEMBLY NO.: 1100-00-2202	REV: C
		PAGE 5	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	SCHOTTKY,15V,20MA				
CR13	BRIDGE ASSY,4 AMP	RS602	DIODE	4899-00-0037	1
Q1 Q2	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	2
SW1	SWITCH PC	240008C	EECO	5199-00-0004	1
VR1 VR3 VR4	VOLT REGULATOR, 3 TERMINAL ADJUSTABLE PDS	LM317T	NSC	7000-03-1700	3
VR2	VOLT REGULATOR	LM337T	NSC	7000-03-3700	1
U16 U19 U20 U26 U27	OP AMP INPUT	TL082CP	TI	7000-08-2000	5
U15	DAC	DAC1006LCN	NAT	7000-10-0600	1
U17	SW, QUAD ANALOG, CMOS	DG211CJ	SLCON	8000-02-1100	1
U7B U8B	BUS XCVR, BIDIR, O, TTL	MC3447P3	MOT	8000-34-4700	2
U11 U12	RAM 2K X 8, CMOS STATIC	CXK5816PN-12L	SONY	8000-61-1600	2
U3	MICROPROCESSOR, 8BIT	MC6803L	MOT	8000-68-0300	1
U1	GATE, NAND, QUAD 2-INP, TTL	SN74LS00N	TI	8000-74-0010	1
U18	INVERTER,HEX, TTL	74LS04	TI	8000-74-0410	1

WAVETEK PARTS LIST	TITLE: ASSY MICRO-PROC/GPIB BOARD	ASSEMBLY NO.: 1100-00-2202	REV: C
		PAGE 6	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, MICRO-PROC/ POWER SUPPLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO: 278	DWG NO: 1100-00-2202 REV: C
	SCALE	CODE IDENT: 23338	SHEET 1 OF 2

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
U2	COUNTER, 12 BIT NIN, CMOS	14040	RCA	8001-40-4000	1
U6	ADPT, GPIB INTERFACE	MC6848P	MOT	8006-84-8800	1
U14	DECODER, DUAL 2-4, TTL	74LS139	SIG	8007-41-3910	1
U5	BUF, OCT 3ST OUT, TTL	M74LS240P	MITSU	8007-42-4010	1
U28 U29	BUF, OCT 3ST OUT, TTL	SN74LS244N	TI	8007-42-4410	2
U25 U4	LATCH, OCTAL TRANSPAR W/3 STATE	74LS373	MOT	8007-43-7310	2
U21 U22 U23 U24	FLIP-FLOP, OCT D, CMOS	MM74C374N	NSC	8007-43-7430	4

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	ASSY MICRO-PROC/GPIB BOARD	1100-00-2202	C

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE				DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES		WAVETEK Wavetek Inc.		
x/x ± 1/64	xxx ± .005	.xx ± .01	∠ ± 1°	DRAWN	DATE	TITLE		
MATERIAL:				CHKD		PARTS LIST PCA, MICRO-PROC/ POWER SUPPLY		
FINISH:				ENG APPR.		SIZE D	MODEL NO 278	DRAWING NO 1100-00-2202 REV C
				MFG APPR		SCALE:	CODE IDENT 23338	SHEET 2 OF 2
				ISSUED				

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	PROM INSTALLATION DRAWING(MICRO-PROC/	0101-00-1025	WVTK	0101-00-1025	1
A6U13	IC, PROGRAMMED REF: 8008-21-0200	8600-00-0237	WVTK	8600-00-0237	1
U9	EPROM, PROGRAMMED SET V2.4 REF: 8000-27-6400	8600-00-0425	WVTK	8600-00-0425	1
U10	EPROM, PROGRAMMED SET V2.4 REF: 8000-27-6400	8600-00-0426	WVTK	8600-00-0426	1

WAVETEK PARTS LIST	TITLE: PROM PACKAGE	ASSEMBLY NO. 1109-00-0021	REV C
		PAGE 1	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PROM PACKAGE
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 278	DWG NO 1109-00-0021 REV C
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

REV	ECN	BY	DATE	APP
/	3369 CLASS III	SC	12282	
A	#3904	SC	7-29-83	
B	ECN 4141	RO	3/84	
C	ECN 4340	RO	9-12-84	
D	#4719	JM	4-5-86	
E	#7757	BR	11/6/86	SS

CONTROL LOGIC

DIGITAL INTERFACE J16-

+5V
R2 2.2K SIP -5 -2 -4 -6 -9 -8 -7 -3 -10
J16- 1 2 3 4 5 6 7 8
ADRØ
ADR1
ADR2
N.C.
N.C.
LOCK DETECT (3B1)
R1 2.2K SIP -8 -4 -7 -2 -6 -5 -3 -9 -10
U1 74LS138 A B C EØ E1 E2 Ø 1 2 3 4 5 6 7 15 14 13 12 11 10
C1 .1/50V
BINARY B(3D7)
BINARY A(3D7)
U2 74C374
U3 74C374
U4 74C374
U5 74C374
U6 74C374
U7 74C374
C2 .1/50V
C3 .1/50V
C4 .1/50V
B7 B6 B5 B4 B3 B2 B1 B0
B15 B14 B13 B12 B11 B10 B9 B8
BURST (B1,B2)
INT/EXT TRIG (3B6)
BURST (B2)
SYNTH Ø SELECT (2A3)
INTERNAL REF (2D8)
REF LEVEL SELECT (2C5)
SYN/REF (3B6)
VCO
VMP3 (2B2)
VMP2 (2B2)
VMP1 (2B2)
VMPØ (2B2)
CLOCK (2B8)
DATA (2B8)
ENABLE (2B8)
(N.C.)
1K-9.99K (3D4)
100K-1.2MHz (3D4)
10K-99.9K (3D4)
1Ø-999Hz (3D4)
DECADE A (3C7)
DECADE B (3C7)
DECADE C (3C7)
1Ø-99.9Hz (3B3)

ANALOG INTERFACE J15-

(3C1)
(3D1)
TRGØ (3B5)
N.C.
SQS (3C5)
U8B 74F00
U8A
C5 .1/50V
C6 .1/50V
U9 74LS161
U10 74LS161
U11 74LS161
U12 74LS161
U13 74LS161
C7 .1/50V
U14 74S133
C8 33pF
74F74 U15A
R3 332
C8 100pF
U15B
BURST (C4)
U8C 74F00
U8D
BURST (C4)
TRGØB (3B5)

BURST COUNTER

AUX POWER J17-

+15V-1 (3B5)
FB1
+15V
C9 100/16V
FB2
-15V
FB3
C10 +100/16V
C11 100/16V
-15V-1 (3A5)

TP7 TP8 TP9 TP10

6. LAST REFERENCE DESIGNATORS USED ARE: R84, C89, CR13, Q5, U48, VR2, FB5
5. DG211 MODE 4 SWITCHES ARE SHOWN FOR FREQUENCY OF 1K
4. ALL DIODES ARE FD 6666.
3. ALL CAPACITORS ARE IN MICRO FARADS.
2. ALL RESISTORS ARE IN OHMS.
1. REFERENCE DESIGNATORS SHOWN ARE PARTIAL PREFIX WITH ASSEMBLY REF DES (A10)

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 22282	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RB4	7/15/83	TITLE SCHEMATIC, SYNTHESIZER BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030	
	DO NOT SCALE DWG	SCALE	MODEL NO. 278 / DWG NO. 0103-00-0978 / REV E
		CODE IDENT 23338	SHEET 1 OF 3

SYNTHESIZER REFERENCE

REV	ECN	BY	DATE	APP

INTERNAL REF (IC4) — R4 10K — CR1 — R5 100K — Q1 2N3646 — +5V — R6 3.32K — CR2 FD777 — +15V — R7 27.4K — R8 10K — C12 180pF SM — C13 3300pF SM — Y1 10MHz XTAL — Q2 2N3563 — R9 6.81K — C14 7-35pF — 10.0 MHz REF ADJ — C15 220pF SM — C16 20pF SM — R29 10K — R10 10K

+5V — C17 .1/50V — U16 NE521

INTERNAL REF (IC4) — U17 A, U17 D, U17 B, U17 C (74LS00) — C22 .1/50V — 10MHz (3B6) — C23 .1/50V

U18 ÷25 (74LS390) — 400KHz — U19 ÷5 (74LS390) — 80KHz — U20 ÷25 (74LS390)

Ø LOCK IN (3C6) — R15 7.87K — REF LEVEL SELECT (IC4)

P13 REF INPUT -4 -3 — W17 — E4 E3 — R11 1K — CR5 IN5282 — CR4 — R12 1K — R13 20K — R14 1.5K — C21 .1/50V

-5Vdc ISO — C18 .1/50V — C19 100/16V

VR1 7905 IN OUT COM — -15VDC — C20 .1/50V

3200Hz

C29 .1 MYLAR — R22 78.7K — C30 5 MYLAR — C31 .1/50V — LF356 U23 — R17 33.2K — R18 33.2K — R19 10K — R20 10K — C32 .1/50V — C26 .1/50V — C27 .1/50V — C28 .1/50V

C35 .001 — R27 499K — C36 .1/50V — LF356 U24 — R25 1.62K — R23 10K — R24 10K — C33 .1/50V — C34 .1/50V — R26 10K — C37 .1/50V — C47 .1/50V

R28 499 — C38 1/35V TANT — C39 .1/50V

FB4 FB5 — C40 .1/50V — L1 — CR6 MV1404 — C41 .1/50V — U25 MC1648 — C42 .1/50V — R30 10K — CR7 — R31 0 — Q3 2N4258 — 20-48MHz — R32 249

C44 .1/50V — U26 74F74 ÷2 — R33 100 — SYNTH/Ø SELECT (IC4)

VCO

74LS02 — U22 A, U22 B, U22 D — R21 1K — C46 220pF — VMP SET (B1)

7805 — +15V — VR2 — +5V ISO — C24 .1/50V — C25 100/16V

INTERNAL SYNTHESIZER LOOP

VMP — 74LS163 U29 — VMPØ (IC3) VMP1 (IC3) VMP2 (IC3) VMP3 (IC3) — C45 .1/50V — 74LS00 U30 B — 74LS163A U28 ÷10/÷11 — U27 A, U27 B (74LS74) — VMP SET (A6) — 1-2.4MHz — Fo (B8) — U30 A — R34 10

VCO (3D8, 3C7) 10M-24MHz

Fo (B1) 1-2.4MHz — TP4 — TP5 — TP6 — U21 145155 — CLOCK (IC3) DATA (IC3) ENABLE (IC3)

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 3-2-82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR RBG	1/18/83	TITLE: SCHEMATIC, SYNTHESIZER BOARD
FINISH WAVETEK PROCESS	RELEASE BY APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 278	DWG NO 0103-00-0978 REV E
	SCALE	CODE IDENT 23338	SHEET 2 OF 3

REV	ECN	BY	DATE	APP

SYNTHESIZER FREQUENCY DIVIDERS

MAIN LOOP

BINARY A (IC6) — BINARY B (IC6) — 74LS163 — U31 — U32 — 74LS151

VCO (2A2) 10M-24MHz — C48 .1/50V — C49 .1/50V — +5V

1-10MHz — 100K-999KHz — 74LS390 — U33 — C50 .1/50V

10K-99.9KHz — 1K-99.9KHz — U34 — 74LS390

100Hz-999Hz — 10Hz-99.9Hz — U35 — 74LS390 — 1Hz-9.99Hz

SYNTH/Ø SELECT (IC4) — VCO (2A2) — DECADE A (IC3) — DECADE B (IC3) — DECADE C (IC3) — U36 74LS151

Ø LOCK IN (2C3) — U37 A/B/C/D — 74LS00 — C55 .1/50V

INT/EXT TRIG (IC4) — TRGO (IB7) — U38 A/B/C/D — 74LS00 — C72 .1/50V — TRGOB (IB3)

SYN/REF (IC4) — 10MHz (2C3) — U39 A/B/C — 74LS00 — C76 .1/50V

100K-12MHz (IC3) — R35 4.99K — C51 .1/50V

10K-99.9K (IC3) — R36 4.99K — C52 .1/50V

1K-9.99K (IC3) — R37 4.99K — C53 .1/50V

10Hz-999Hz (IC3) — R38 4.99K — C54 .1/50V

+15V DG211 -15V — U43 — C75 .1/50V

TP3 — U42 7416 — U41 MC4044 — U40 A 74LS574 — SQ5 (IB8) — U40 B 74LS574

C61 .1/50V — C56 .1/50V — C57 .1/50V — C58 .1/50V — R43 10 — +15VDC — R47 78.7K — R46 12.4K — U43A DG211 — R44 2.49K — R45 12.4K — CR8 — CR9 HP2811(A) — CR10 — CR11

R48 15K — U43B DG211 — R50 78.7K — R49 15K — -15VDC — 10-99.9Hz (IC2)

U45A DG211 — U45D — U45C — U45B — CG2 100pF SM — CG3 .01 MYLAR — R39 16.5K — CG4 .001 MYLAR — R40 49.9K — CG5 .1 MYLAR — CG6 .01 MYLAR — R41 49.9K — CG7 1.0 MYLAR — CG8 .1/50V — R42 49.9K — CG9 5.0 MYLAR

+15V DG211 -15V — U45 — +5V

R54 49.9K — C74 .1/50V — LF356 — U44 — R51 4.99K — R52 10K — C60 .1/50V — R53 10K — C73 .1/50V — R55 100 — C71 100pF — -15V

R56 24.9K — R57 24.9K — U47C DG211 — C70 100pF — U47D DG211 — LF356 — U48 — R58 2K — R59 20K — VCGO J15-4 (IC8) — +15VDC — J15-2 (IC8) — TP1 — TP2 — -15V — +15V VCGI — C89 .1/50V — C88 .1/50V

R61 49.9K — R62 8.25K — R67 10K — LM393 — U46A — R64 100K — R63 10K — C85 .1/50V — C87 .1/50V — U47A DG211 — R60 10K — VCG/ (IC4) — +5V

+15V DG211 -15V — U47 — +5V

LM393 — U46B — R65 10K — R66 2.49K — C86 .1/50V — LOCK DET (IC8)

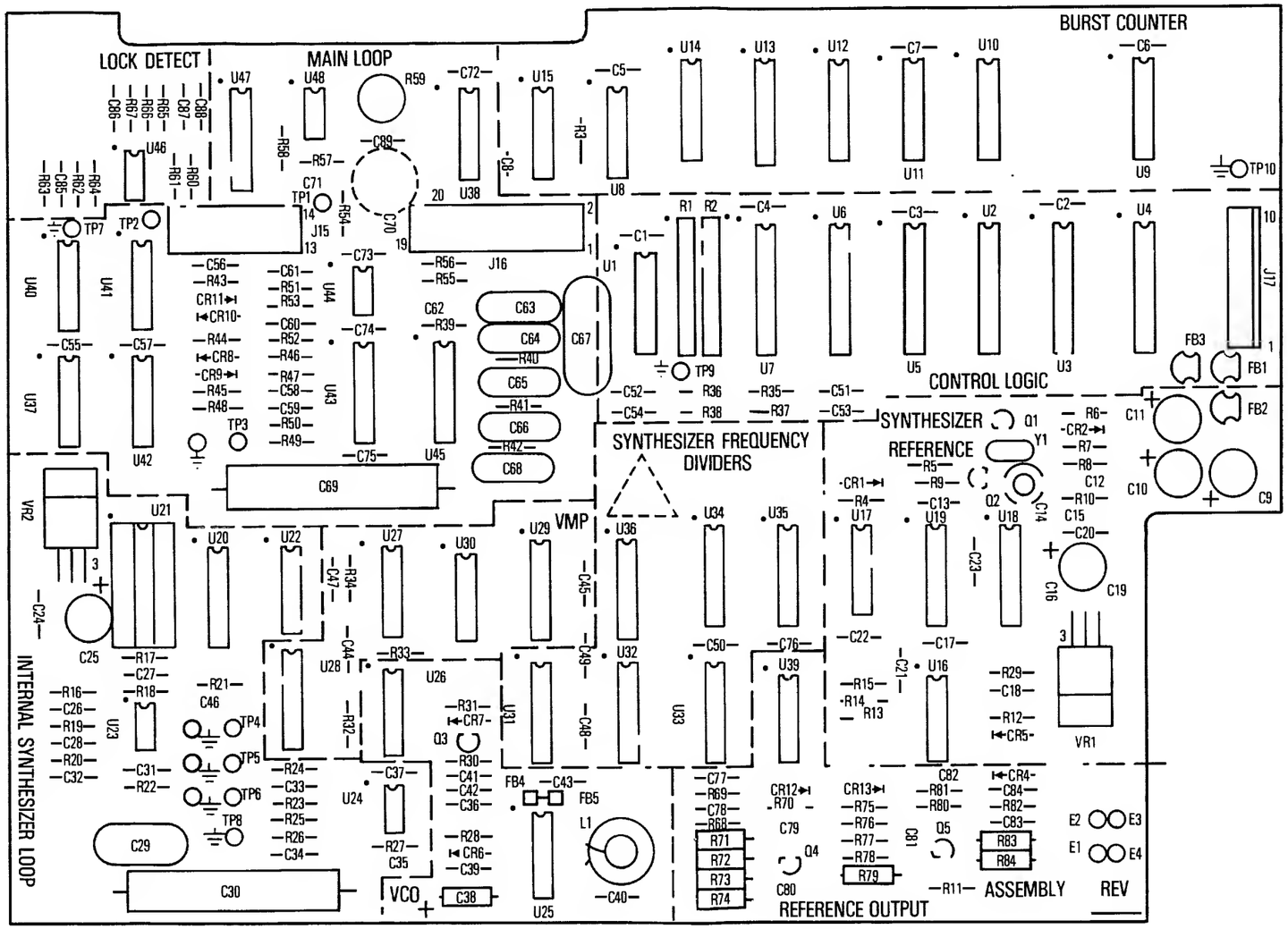
620,1/2W (4) — +15V-1 (IA5) — C77 .1/50V — C78 .1/50V — R68 2.49K — R69 2.49K — C79 100pF — R70 249 — R71 — R72 — R73 — R74 — C80 .001 — Q4 2N2369A — CR12 — R75 10 — R76 10 — R79 43,1/2W — C81 100pF — R77 10 — R78 10 — CR13 — R80 249 — Q5 2N4122 — C82 .001 — C83 .1/50V — R81 2.49K — R82 2.49K — R83 620,1/2W — R84 620,1/2W — -15V-1 (IA5) — C84 .1/50V

E1 — W16 — E2 — P13 -1 — -2 — REF OUTPUT

REFERENCE OUTPUT — LOCK DETECT

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 3-2-82	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR KBG	7/15/83	TITLE: SCHEMATIC, SYNTHESIZER BOARD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		
	SCALE	MODEL NO. 278	DWG NO. 0103-00-0978 REV E.
		CODE IDENT 23338	SHEET 3 OF 3



MADE FROM 0100-00-0978-3H

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: SYNTHESIZER BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ·010 ANGLES ·1 XX ·030		
	DO NOT SCALE DWG	MODEL NO 278	DWG NO 1100-00-0978 REV
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY ORWG, SYNTH BD	0101-00-0978	WVTK	0101-00-0978	1
NONE	SCHEMATIC, SYNTH BD	0103-00-0978	WVTK	0103-00-0978	1
L1	COIL, VCO	27B-0053	WVTK	1204-00-0053	1
NONE	ASSY, AUX BD SHIELD	27D-1038	WVTK	1206-00-1038	1
NONE	SHIELD, COIL	270-5421	WVTK	1400-01-5421	1
C70 C71 C79 C8 C81	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	5
C35 C80 C82	CAP, CER, .01MFD, 1KV	DD-102	CRL	1500-01-0211	3
C1 C17 C18 C2 C20 C21 C22 C23 C24 C26 C27 C28 C3 C31 C32 C33 C34 C36 C37 C39 C4 C40 C41 C42 C43 C44 C45 C47 C48 C49 C5 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C6 C60 C61 C7 C72 C73 C74 C75 C76 C77 C78 C83 C84 C85 C86 C87 C88 C89	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	59
C46	CAP, CER, 220PF, 1KV	DD-221	CRL	1500-02-2111	1
C62	CAP, MICA, 100PF, 500V	DM15-101J	ARCO	1500-11-0100	1
C12	CAP, MICA, 180PF, 500V	DM15-181J	ARCO	1500-11-8100	1
C16	CAP, MICA, 20PF, 500V, RADIAL	DM15-200J	ARCO	150D-12-0000	1

WAVETEK PARTS LIST | TITLE: PCA, SYNTHESIZER BD | ASSEMBLY NO. 1100-00-0978 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SOCKET, 18 PIN	DILB18P-108T	BURND	2100-03-0050	1
NONE	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	6
Y1	CRYSTAL, 10MHZ	2300-99-0007	SAVOY	2300-99-0007	1
NONE	TIE MOUNT	TM-256C	PANDT	2800-00-0005	1
NONE	MNTG CLIP, CABLE TIE	SNF-2	WKESR	2800-00-0031	1
FB4 FB5	FERRITE BEAD	56-590-65/3B	FERRX	3100-00-0001	2
FB1 FB2 FB3	BALUN CORE	2873000902	FARIT	3100-00-0002	3
NONE	INSULATOR, MICA	64-21-023-106	ASHVL	3100-00-0006	2
R59	POT, TRIM, 20K	91AR20K	BECK	4600-02-0301	1
R79	RES, C, 1/2W, 5%, 43	RCR206430JS	AB	4700-25-0430	1
R71 R72 R73 R74 R83 R84	RES, C, 1/2W, 5%, 620	RC-1/2-621J	STKPL	4700-25-6200	6
R16 R33 R55	RES, MF, 1/8W, 1%, 100	RN550-1000F	TRW	4701-03-1000	3
R11 R12 R21	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	3
R10 R19 R20 R23 R24 R26 R29 R30 R4 R52 R53 R60 R63 R65 R67 R8	RES, MF, 1/8W, 1%, 10K	RN550-1002F	TRW	4701-03-1002	16
R5 R64	RES, MF, 1/8W, 1%, 100K	RN550-1003F	TRW	4701-03-1003	2
R34 R43 R75 R76 R77 R78	RES, MF, 1/8W, 1%, 10	RN55010R0F	MEPCO	4701-03-1009	6

WAVETEK PARTS LIST | TITLE: PCA, SYNTHESIZER BD | ASSEMBLY NO. 1100-00-0978 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R40 R41 R42 R54 R61	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	5
R9	RES, MF, 1/8W, 1%, 6.81K	RN550-6811F	TRW	4701-03-6811	1
R15	RES, MF, 1/8W, 1%, 7.87K	RN550-7871F	TRW	4701-03-7871	1
R22 R47 R50	RES, MF, 1/8W, 1%, 78.7K	RN550-7872F	TRW	4701-03-7872	3
R62	RES, MF, 1/8W, 1%, 8.25K	RN55D-8251F	TRW	4701-03-8251	1
R1 R2	RES NETWORK 2.2K 2% 10PIN SIP BUSS	4310R-101-222	BOURN	4770-00-0011	2
R31	RES, 0 OHM JUMPER	JP02T6BQ	ROHM	4799-00-0087	1
CR5	DIODE, HIGH CONDUCTANCE, ULTRA FAST	1N5282	FAIR	4801-01-5282	1
CR6	DIODE, HIGH CAP TUNING	MV1404	MOT	4803-02-1404	1
CR2	DIODE, ULTRA FAST	FD777	FAIR	4807-02-0777	1
CR1 CR12 CR13 CR4 CR7	DIODE 1N4148 COMPUTER, G/P, 75V, 200MA, SWITCHING	1N4148	FAIR	4807-02-6666	5
CR10 CR11 CR8 CR9	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	4
Q4	TRANS, SILICON PLANAR, EPITAXIAL NPN	2N2369A	MOT	4901-02-3691	1

WAVETEK PARTS LIST | TITLE: PCA, SYNTHESIZER BD | ASSEMBLY NO. 1100-00-0978 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C15	CAP, MICA, 220PF, 500V, RADIAL	DM15-221J	ARCO	1500-12-2100	1
C13	CAP, MICA, 3300PF, 500V	DM19-332J	ARCO	1500-13-3200	1
C10 C11 C19 C25 C9	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	ULB1V101M	NICH	1500-31-0102	5
C64	CAP, MYLAR, .001MF100V	225P10291WD3	SPRAG	1500-41-0204	1
C63 C66	CAP, MYLAR, .01MF, 100V	225P10391WD3	SPRAG	1500-41-0314	2
C29 C65 C68	CAP, MYLAR, .1MF, 100V	225P10491WD3	SPRAG	1500-41-0444	3
C67	CAP, MYLAR, 1MF, 100V, RADIAL	PMT2R1.0K100	1TT	1500-41-0524	1
C30 C69	CAP, POLYC, 5MF, 100V	C1A505F	ELPAC	1500-45-0504	2
C14	CAP, VAR, 7-35PF 250V	7S-TRIKO-02 7/35 PF	TRIKO	1500-53-5000	1
C38	CAP, TANT, 1MF, 35V	1500105X9035A2	SPRAG	1500-71-0502	1
NONE	SYNTHESIZER BOARD	270-0978	WVTK	1700-00-0978	1
NONE	CONN, HEADER, 10 PIN	1-640456-0	AMP	2100-02-0133	1
J15	CONN, HOUSING, 14 PIN WITH POLARIZING TABS	2100-02-0136	WVTK	2100-02-0136	1
J16	CONN, HOUSING, 20 PIN WITH POLARIZING TABS	2100-02-0137	WVTK	2100-02-0137	1

WAVETEK PARTS LIST | TITLE: PCA, SYNTHESIZER BD | ASSEMBLY NO. 1100-00-0978 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R45 R46	RES, MF, 1/8W, 1%, 12.4K	RN550-1242F	TRW	4701-03-1242	2
R14	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	1
R48 R49	RES, MF, 1/8W, 1%, 15K	RN550-1502F	TRW	4701-03-1502	2
R25	RES, MF, 1/8W, 1%, 1.62K	RN550-1621F	TRW	4701-03-1621	1
R39	RES, MF, 1/8W, 1%, 16.5K	RN550-1652F	TRW	4701-03-1652	1
R58	RES, MF, 1/8W, 1%, 2K	RN550-2001F	TRW	4701-03-2001	1
R13	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	1
R32 R70 R80	RES, MF, 1/8W, 1%, 249	RN550-2490F	TRW	4701-03-2490	3
R44 R66 R68 R69 R81 R82	RES, MF, 1/8W, 1%, 2.49K	RN550-2491F	TRW	4701-03-2491	6
R56 R57	RES, MF, 1/8W, 1%, 24.9K	RN550-2492F	TRW	4701-03-2492	2
R7	RES, MF, 1/8W, 1%, 27.4K	RN55D-2742F	TRW	4701-03-2742	1
R6	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	1
R17 R18	RES, MF, 1/8W, 1%, 33.2K	RN550-3322F	TRW	4701-03-3322	2
R3	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1
R28	RES, MF, 1/8, 1%, 499	RN550-4990F	TRW	4701-03-4990	1
R27 R35 R36 R37 R38 R51	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	6

WAVETEK PARTS LIST | TITLE: PCA, SYNTHESIZER BD | ASSEMBLY NO. 1100-00-0978 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q2	TRANS, NPN, TO-92	2N3563	FAIR	4901-03-5630	1
Q1	TRANS, NPN, -TO-92	MPS3646	MOT	4901-03-6460	1
Q5	TRANS, GENERAL PURPOSE, PNP, TO-92	2N4122	NSC	4901-04-1220	1
Q3	TRANS, PNP, TO-92	MPS-L0B	FAIR	4902-00-0080	1
W15	RIBBON CABLE (3 INCH)	6002-00-0018	WVTK	6002-00-0018	1
W13	RIBBON CABLE (7 INCH)	6002-00-0019	WVTK	6002-00-0019	1
U23 U24 U44 U48	OP-AMP	LF356N	NSC	7000-03-5600	4
U46	COMPARATOR, LOW POWER LOW OFFSET VOLTAGE DUAL	LM393N	NSC	7000-03-9300	1
U16	COMPARATOR, DUAL DIFFERENTIAL, SENSE AMP	NE521	SIG	7000-05-2100	1
VR1	VOLT REGULATOR, NEGATIVE	MC7905CP	MOT	7000-79-0500	1
U43 U45 U47	SW, QUAD ANALOG, CMOS	DG211CJ	SLCON	8000-02-1100	3
U8	GATE, NAND, QUAD 2INP, TTL	74F00PC	FAIR	8000-74-0002	1
U17 U30 U37 U38 U39	GATE, NAND, QUAD 2-INP, TTL	SN74LS00N	TI	8000-74-0010	5

WAVETEK PARTS LIST | TITLE: PCA, SYNTHESIZER BD | ASSEMBLY NO. 1100-00-0978 | REV C

NOTE. UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, SYNTHESIZER BD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 278 / DWG NO. 1100-00-0978 / REV C
	SCALE		CODE IDENT 23338 / SHEET 1 OF 2

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U22	GATE, NOR, QUAD, 2INP, TTL	74LS02	TI	8000-74-0210	1
U42	INVERTER BUFRS/DRVRS, HEX, W/OC HIGH VOLT O/P	7416	SIG	8000-74-1600	1
U15 U26	FLIP-FLOP DUAL, D-POS EDGE TRIG, TTL	74F74PC	FAIR	8000-74-7402	2
U27 U40	FLIP-FLOP DUAL, D-POS EDGE TRIG, TTL	74LS74	TI	8000-74-7410	2
VR2	VOLT REGULATOR	MA7805UC	FAIR	8000-78-0500	1
U14	GATE NAND 13-INPUT POSITIVE	74S133	TI	8007-41-3301	1
U1	DECODER, 3-8 LINE, TTL	74LS138	TI	8007-41-3810	1
U32 U36	MUX, DATA, 1 OF 8, TTL	74LS151	TI	8007-41-5110	2
U10 U11 U12 U13 U9	COUNTER, SYNC 4B, TTL	74LS161	SIG	8007-41-6110	5
U29 U31	COUNTER, SYNC 4-BIT, TTL	74LS163	SIG	8007-41-6310	2
U28	COUNTER, SYNC 4 BIT DECADE	SN74ALS163AN	TI	8007-41-6311	1
U2 U3 U4 U5 U6 U7	FLIP-FLOP, OCT D, CMOS	MM74C374N	NSC	8007-43-7430	6

WAVETEK PARTS LIST | TITLE: PCA, SYNTHESIZER BD | ASSEMBLY NO. 1100-00-0978 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U18 U19 U20 U33 U34 U35	COUNTER, DUAL 4B BCD, TTL	74LS390PC	FAIR	8007-43-9010	6
U21	SYNTH, PLL FREQ, CMOS	MC145155	MOT	8100-00-0007	1
U25	OSC EXT CUPLD, ECL	MC1648P	MOT	8100-16-4810	1
U41	IC	MC4044P	MOT	8100-40-4400	1

WAVETEK PARTS LIST | TITLE: PCA, SYNTHESIZER BD | ASSEMBLY NO. 1100-00-0978 | REV C

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS | DRAWN | DATE | PROJ ENGR | RELEASE APPROV | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030 | DO NOT SCALE DWG | SCALE

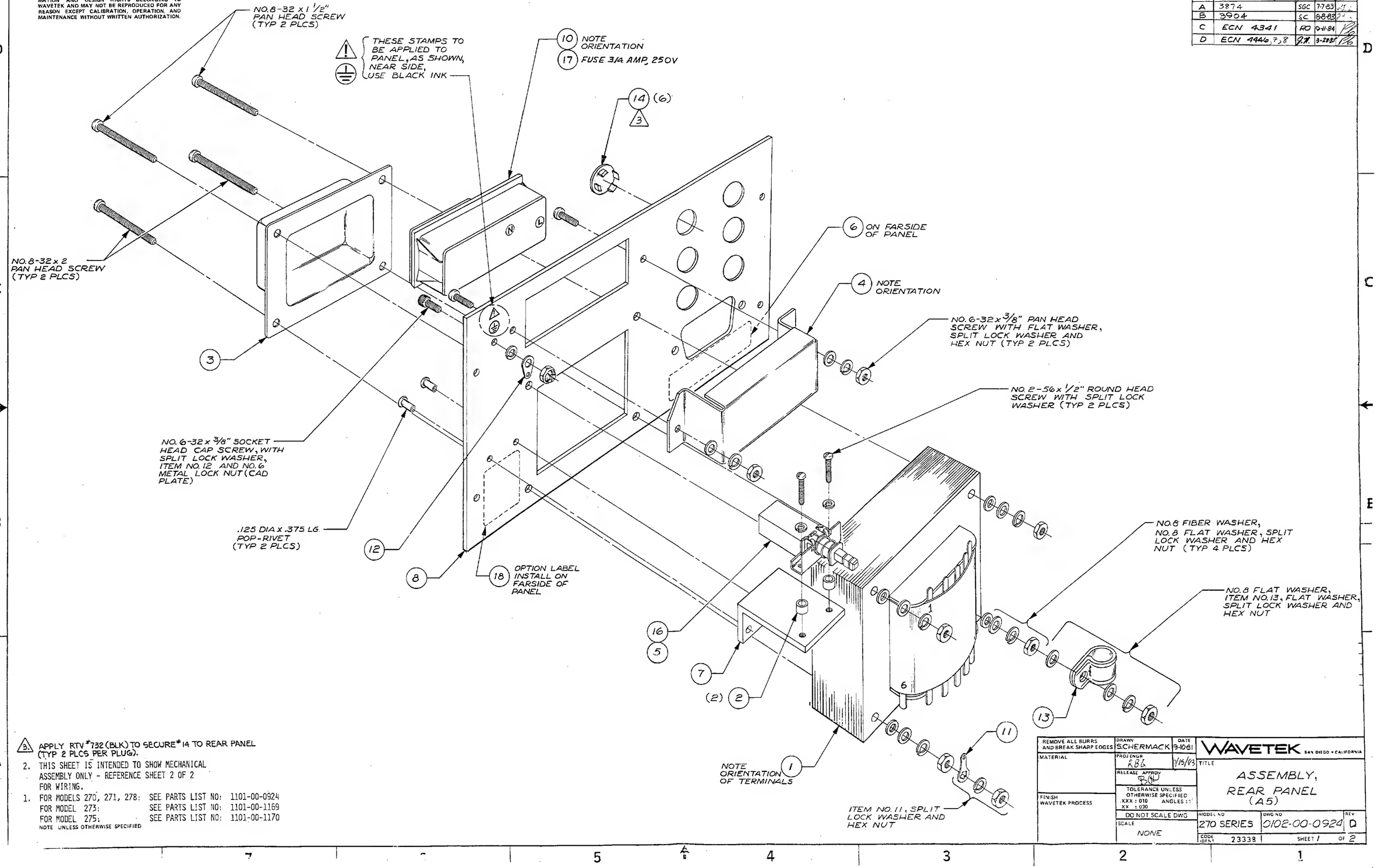
WAVETEK SAN DIEGO, CALIFORNIA

TITLE: PARTS LIST PCA, SYNTHESIZER BD

MODEL NO 278 | DWG NO 1100-00-0978 | REV C | CODE IDENT 23338 | SHEET 2 OF 2

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP
/	3756 (CL II)	fpa	5/11/82	LJC
/	3770 (CL E)	fpa	5/19/82	JHP
A	3874	SGC	7-7-83	JHP
B	3904	SC	8-8-83	JHP
C	ECN 4341	RO	9-11-84	JHP
D	ECN 4446, 7, 8	GH	3-28-85	JHP

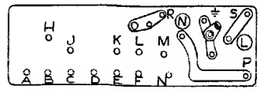


3. APPLY RTV*732 (BLK) TO SECURE*14 TO REAR PANEL (TYP 2 PLCS PER PLUG).
2. THIS SHEET IS INTENDED TO SHOW MECHANICAL ASSEMBLY ONLY - REFERENCE SHEET 2 OF 2 FOR WIRING.
1. FOR MODELS 270, 271, 278: SEE PARTS LIST NO: 1101-00-0924
   FOR MODEL 273: SEE PARTS LIST NO: 1101-00-1169
   FOR MODEL 275: SEE PARTS LIST NO: 1101-00-1170

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN SCHERMACK	DATE 9-10-81	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/15/93	TITLE ASSEMBLY, REAR PANEL (A5)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 0102-00-0924 REV D
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 2

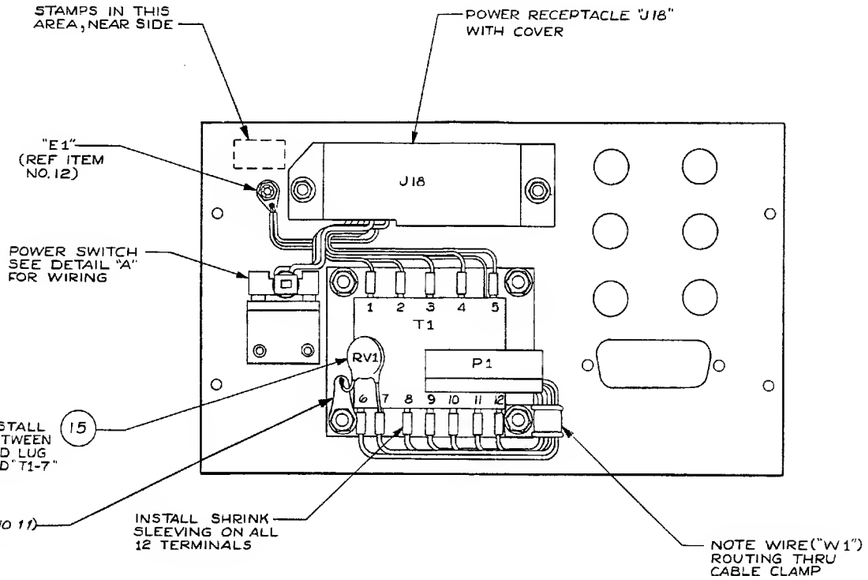
REV	ECN	BY	DATE	APP

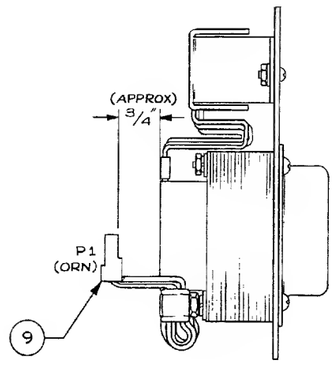


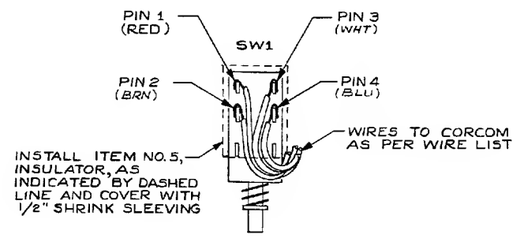
POWER RECEPTACLE PIN MARKING

WIRE LIST

AWG	COLOR	LENGTH	DESTINATION FROM	DESTINATION TO	
18	BLU	4	P1-1	T1-11	W1
18	BLU	4	P1-2	T1-12	
18	GRN	5 1/2	P1-3	T1-6	
18	GRN	5 1/4	P1-4	T1-8	
18	WHT	5 1/2	P1-5	T1-7	
			P1-6		
			P1-7		
			P1-8		
18	RED	5 1/2	P1-9	T1-9	
18	RED	5 1/4	P1-10	T1-10	
22	BLK		J18-C	T1-1	
22	ORN		J18-A	T1-2	
22	WHT/BLK		J18-E	T1-3	
22	GRY		J18-D	T1-4	
22	WHT/GRY		J18-F	T1-5	
22	GRN/YEL		A5-E1	T1(SHIELD)	
22	BUS		J18-B	J18-H	
22	BRN		J18-R	SW1-2	
22	RED		J18-S	SW1-1	
22	BLU		J18-L	SW1-4	
22	WHT		J18-P	SW1-3	
22	GRN/YEL		J18-⏚	A5-E1	

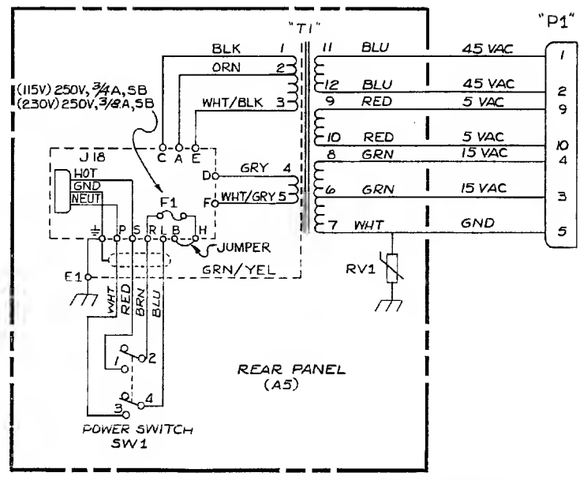






DETAIL "A"

POWER SWITCH WIRING AND INSULATOR ASSY



NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 11-5-81	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/16/83	TITLE: ASSEMBLY, REAR PANEL (A5)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 0102-00-0924 REV D
	SCALE	CODE IDENT 23338	SHEET 2 OF 2

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, REAR PANEL	0102-00-0924	WVTK	0102-00-0924	1
1	TRANSFORMER	270-0049	WVTK	1204-00-0049	1
2	SPACER	8480	WVTK	1400-00-0653	2
3	END BELL	157-500-EB	WVTK	1400-00-3224	1
4	SHIELD, PWR	801-6210	WVTK	1400-00-6210	1
5	INSULATOR, PWR SWITCH REF: 1600-99-0001	801-8370	WVTK	1400-00-8370	1
6	I.D. LABEL	801-9090	WVTK	1400-00-9090	1
7	BRACKET, SWITCH MNTG	189-3263	WVTK	1400-01-3263	1
8	REAR PANEL FROM: 1400-01-3882	270-3880	WVTK	1400-01-3880	1
18	LABEL, OPTION	270-4960	WVTK	1400-01-4960	1
9	CONNECTOR, HOUSING 18 AWG	1-640431-0	AMP	2100-02-0115	1
10	RECEPTACLE	6VJ1	CORCM	2100-03-0026	1
11	TERM, LOCK LUG	1414-B	SMITH	2100-04-0010	1
12	SOLDER LUG	11A144	ZIER	2100-04-0025	1
17	FUSE, 3/4A, 250V, S-B	313-750	LITFU	2400-05-0011	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	ASSY, REAR PANEL	1101-00-0924	B

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
13	CLAMP, CABLE	833	SMITH	2800-00-0022	1
14	PLUG BUTTON MATTE FINISH	62PP050BM14 BLK	MICRO	2800-35-0005	6
15	VARISTOR	4899-00-0045	WVTK	4799-00-0048	1
16	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1

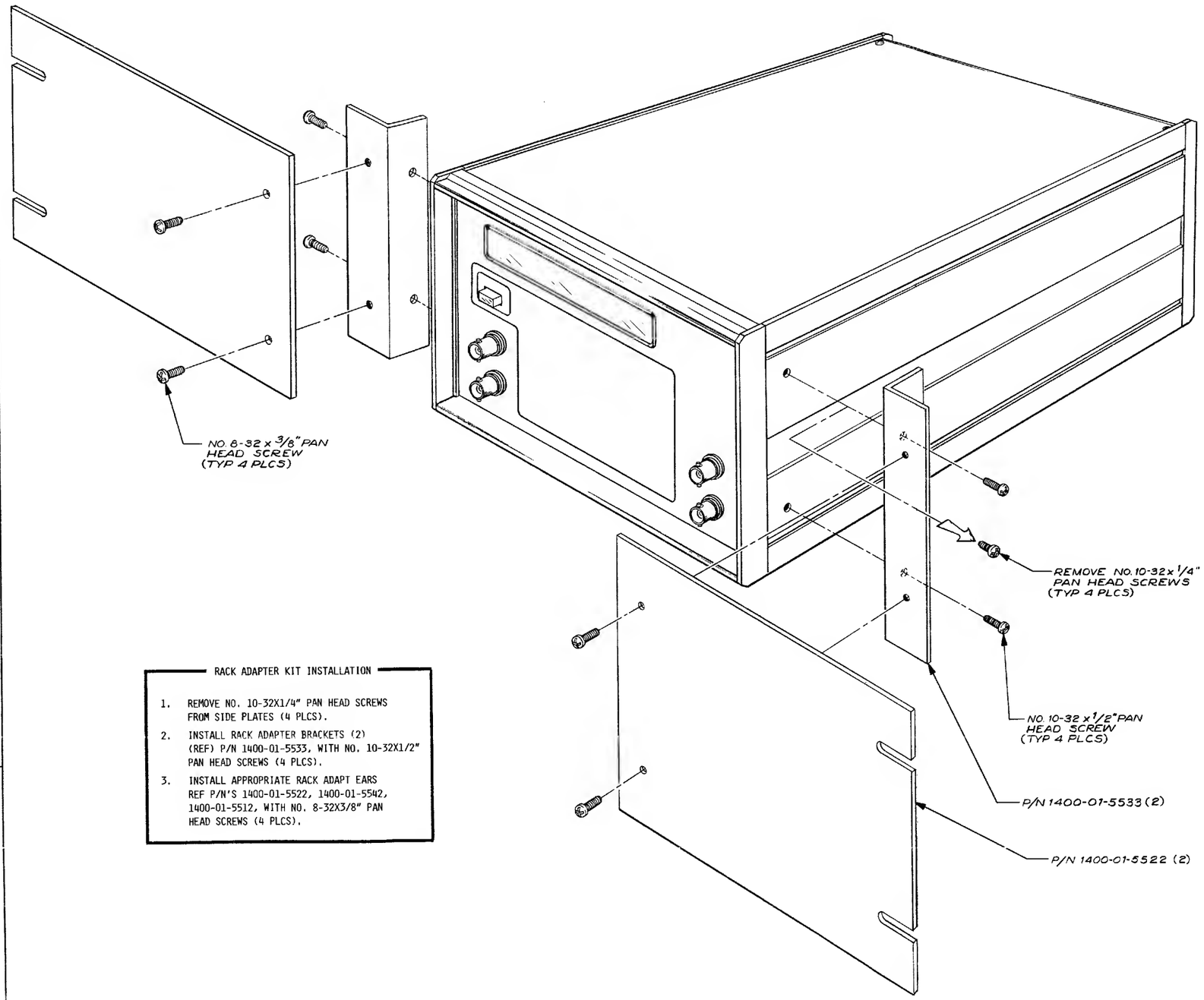
WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	ASSY, REAR PANEL	1101-00-0924	B

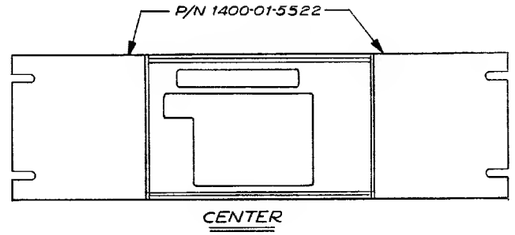
PAGE 2

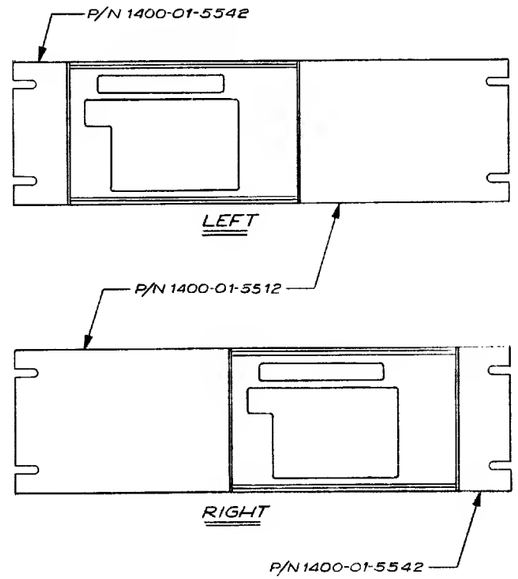
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST ASSY, REAR PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 1101-00-0924 REV B
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	# 3332	SC	7/14/82	







RACK ADAPTER KIT INSTALLATION

1. REMOVE NO. 10-32X1/4" PAN HEAD SCREWS FROM SIDE PLATES (4 PLCS).
2. INSTALL RACK ADAPTER BRACKETS (2) (REF) P/N 1400-01-5533, WITH NO. 10-32X1/2" PAN HEAD SCREWS (4 PLCS).
3. INSTALL APPROPRIATE RACK ADAPT EARS REF P/N'S 1400-01-5522, 1400-01-5542, 1400-01-5512, WITH NO. 8-32X3/8" PAN HEAD SCREWS (4 PLCS).

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 9/1982	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RBG	9/15/82	TITLE ASSEMBLY, RACK ADAPTER KIT
	RELEASE APPROV BOH		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 270 SERIES / DWG NO 0102-00-1043 / REV A
	SCALE NONE		CODE IDENT 23338 / SHEET 1 OF 1

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, RACK ADAPTER KIT, SINGLE	0102-00-1043	WVTK	0102-00-1043	1
NONE	EAR, RACK ADAPT	270-5512	WVTK	1400-01-5512	1
NONE	EAR, RACK ADAPT	270-5522	WVTK	1400-01-5522	2
NONE	ANGLE BRACKET, RACK ADAPT, SINGLE	270-5533	WVTK	1400-01-5533	2
NONE	EAR, RACK ADAPT	270-5542	WVTK	1400-01-5542	1
NONE	SCREW, 10-32X5/8, PHP, Z	10-32 X 5/8 PAN	CMRCL	2800-38-0110	4
NONE	SCREW, PAN, CAD I, CROSS RECESS, 8-32 X 3/8	8-32 X 3/8 PAN	CMRCL	2800-38-8106	4
NONE	#10 LOCKWASHER, PLATED	#10 REG	CMRCL	2800-42-0000	4
NONE	LOCKWASHER, #8 SPLIT RING BIN 540	#8SRLW	CMRCL	2800-42-8000	4

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	R/M STYLE 12, LEFT, CENTER, RIGHT R/M, 270 SERIES	1101-00-1043	A

PAGE 1

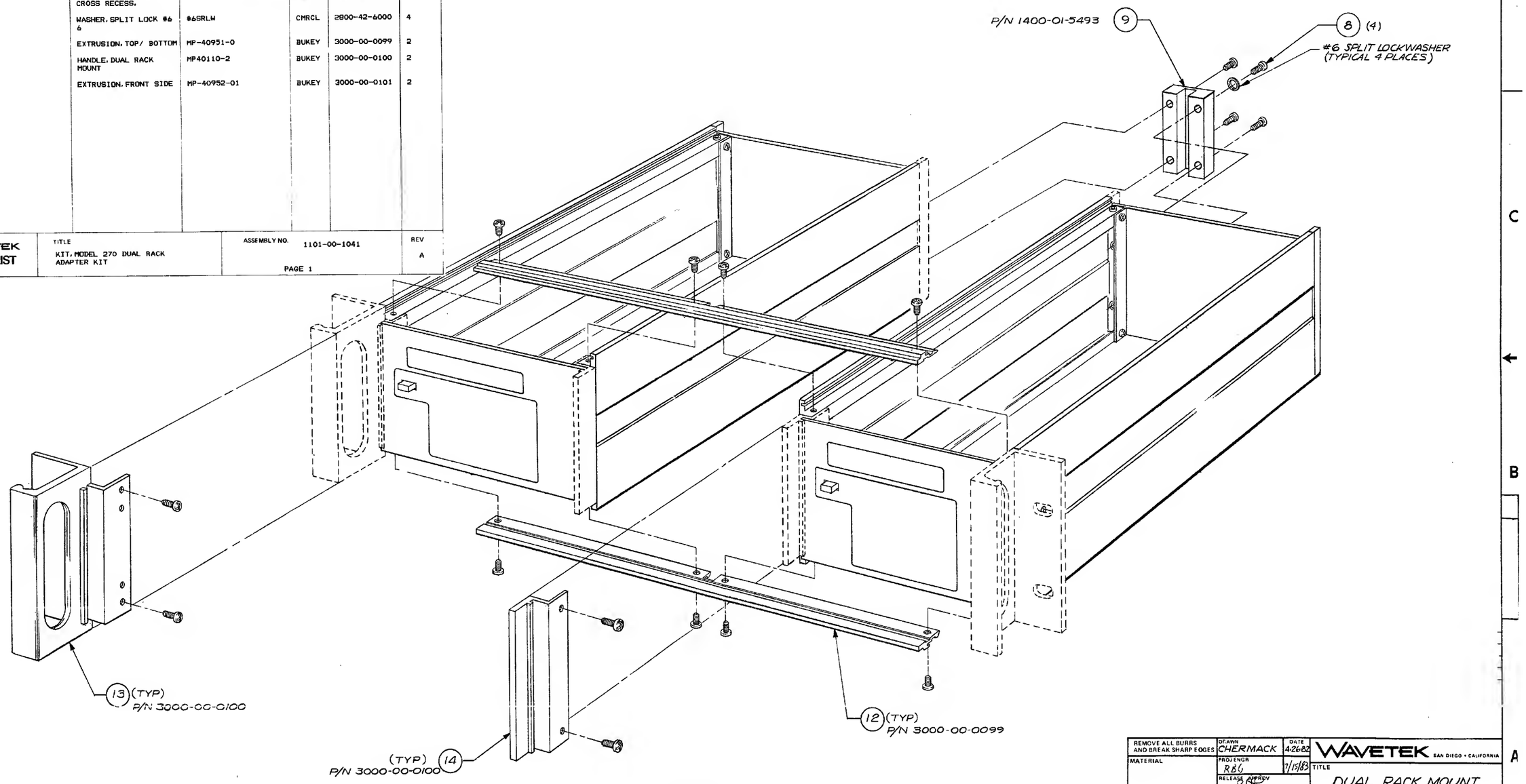
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST MODEL 270 SERIES RACK ADAPTER KIT
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 1101-00-1043 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	ECN 4090	RO	3/84	RB

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, DUAL RACK/ ADAPTER	0102-00-1041	WVTK	0102-00-1041	1
NONE	JOINER, REAR PANEL	270-5493	WVTK	1400-01-5493	1
NONE	SCREW, PAN, CAD I CROSS RECESS,	6-32 X 3/4 PAN	CMRCL	2800-38-6112	4
NONE	WASHER, SPLIT LOCK #6 6	#6SRLW	CMRCL	2800-42-6000	4
NONE	EXTRUSION, TOP/ BOTTOM	MP-40951-0	BUKEY	3000-00-0099	2
NONE	HANDLE, DUAL RACK MOUNT	MP40110-2	BUKEY	3000-00-0100	2
NONE	EXTRUSION, FRONT SIDE	MP-40952-01	BUKEY	3000-00-0101	2

WAVETEK PARTS LIST | TITLE: KIT, MODEL 270 DUAL RACK ADAPTER KIT | ASSEMBLY NO. 1101-00-1041 | REV A

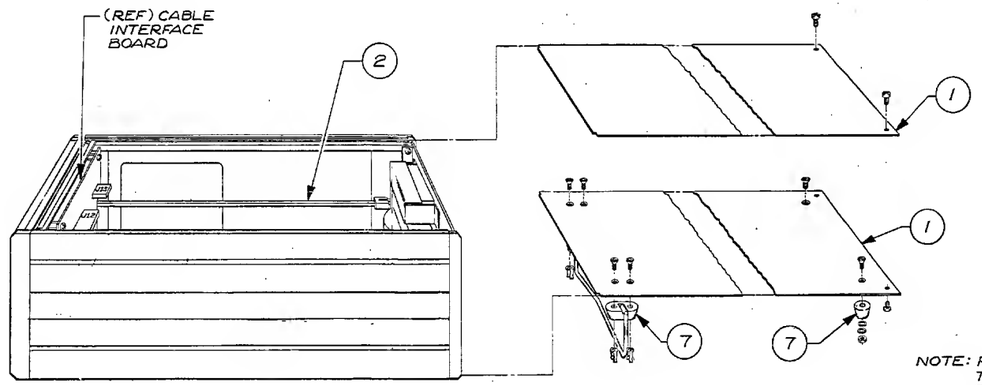


VIEW "A"

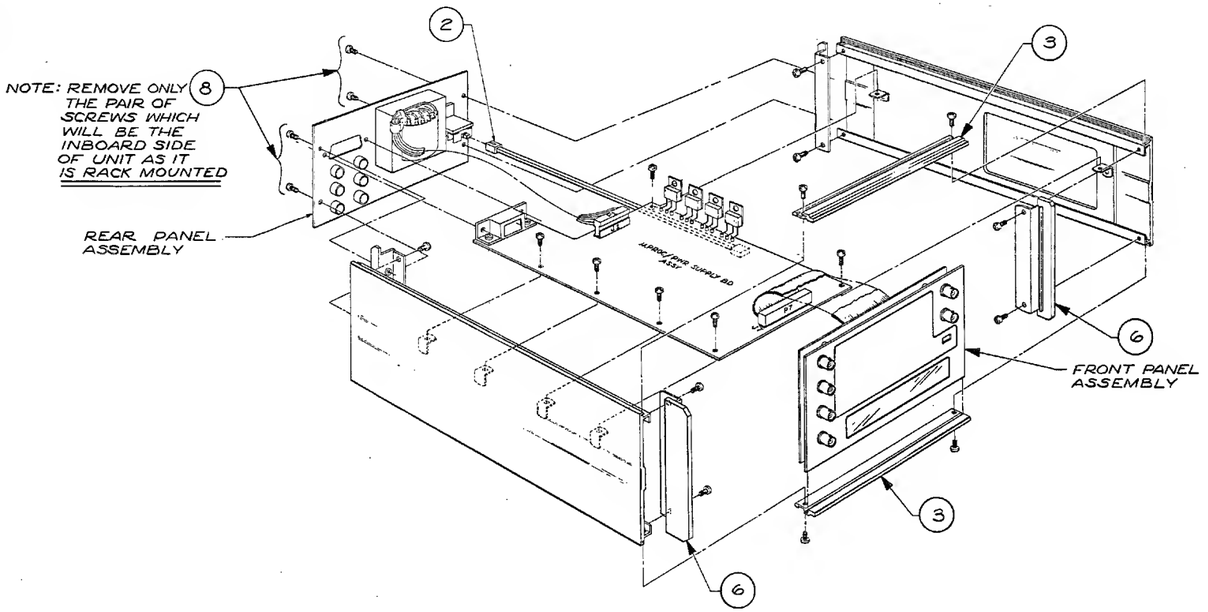
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 4-26-82	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RBO	7/15/83	TITLE: DUAL RACK MOUNT, 270 SERIES
FINISH WAVETEK PROCESS	RELEASE APPROV	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES ± 1° .XX ± .030	
	DO NOT SCALE DWG		MODEL NO. 270 SERIES / DWG NO. 0102-00-1041 / REV A
	SCALE NONE		CODE IDENT 23338 / SHEET 1 OF 2

REV	ECN	BY	DATE	APP



VIEW "B"



VIEW "C"

VIEW "C" IS SHOWN WITH UNIT UPSIDE DOWN.

SEQUENCE OF CHANGES FOR DUAL RACK-MOUNTING (USE ORIGINAL SCREWS EXCEPT ITEM 9.)

1. REMOVE TOP AND BOTTOM COVERS (REF ITEMS #1)
2. REMOVE POWER ROD ASSEMBLY (REF ITEM #2) THRU FRONT PANEL ASSEMBLY.
3. REMOVE BOTH TOP AND BOTTOM FRONT HORIZONTAL TRIM PIECES (REF ITEMS #3) TO BE REPLACED BY NEW TRIM (REF ITEMS #12).
4. DISCONNECT PLUGS, "P12" (AND "P13" IF APPLICABLE) FROM CABLE INTERFACE BD., ALSO DISCONNECT "P7" FROM MICROPROC/POWER SUPPLY BOARD.
5. REMOVE FRONT PANEL ASSEMBLY.
6. REMOVE FRONT VERTICAL TRIM PIECES (REF ITEMS #6) AND REPLACE WITH APPROPRIATE REPLACEMENTS (REF ITEM #'S 13 AND 14).
7. REMOVE FEET AND BAIL ASSEMBLY (REF ITEMS #7) FROM BOTTOM COVER, AND REASSEMBLE BY REVERSING STEPS 1 THROUGH 6.
8. REMOVE APPROPRIATE (INBOARD ONLY) REAR PANEL MOUNTING SCREWS (REF ITEMS #8).
9. INSTALL NEW VERTICAL BRACKET (REF ITEM #9) TO REAR PANELS OF UNITS ON INBOARD MOUNTING HOLES, USING SUPPLIED 6-32 x 3/4 SCREWS AND #6 LOCKWASHER.

VIEWS ARE SHOWN TO ILLUSTRATE MECHANICAL BUILD UP OF UNIT PERTAINING TO ITEMS WHICH MUST BE REMOVED AND REPLACED BY NEW ITEMS TO MAKE A DUAL RACK MOUNT SET UP.

NOTE: UNLESS OTHERWISE SPECIFIED

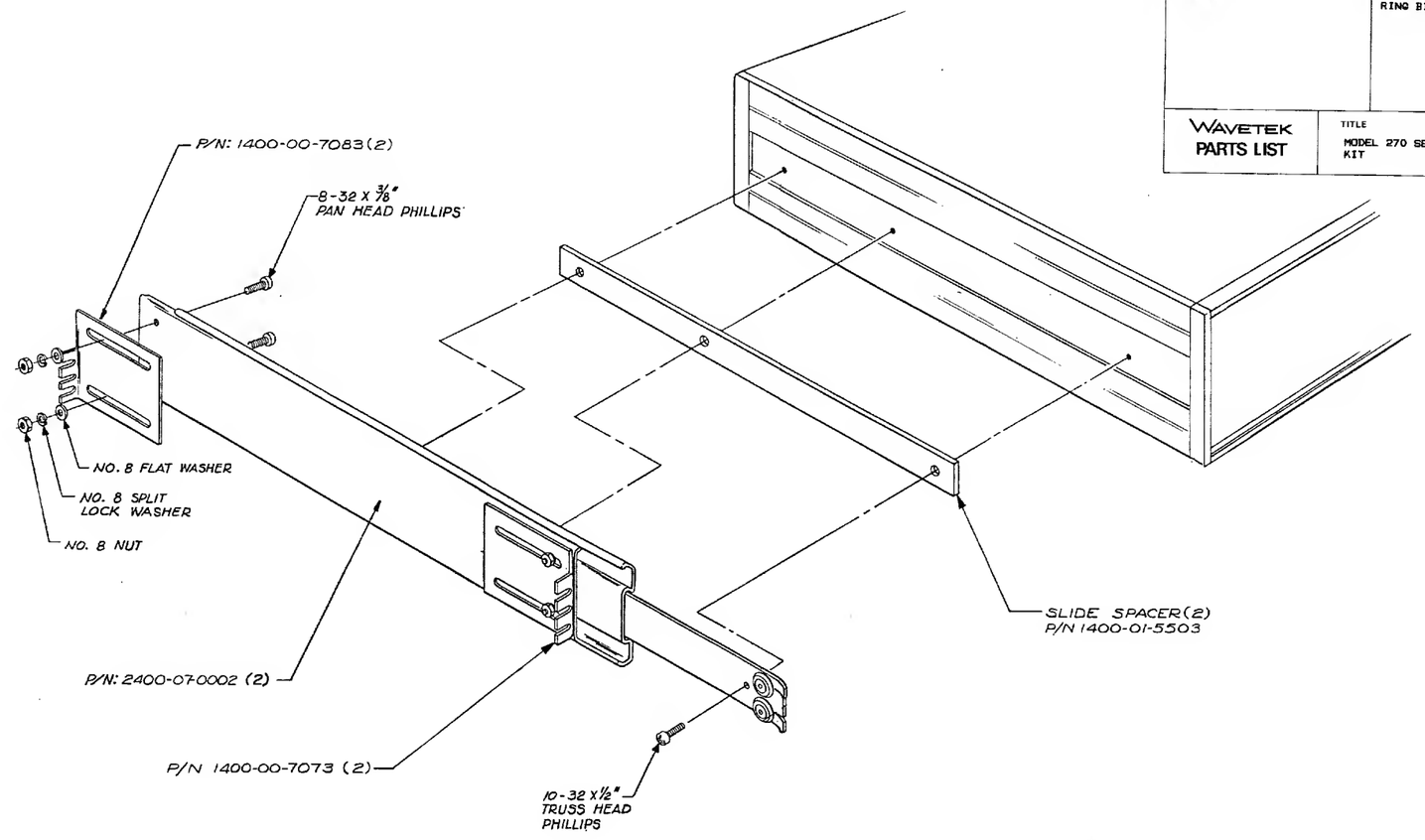
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 4/26/82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/15/83	TITLE: DUAL RACK MOUNT 270 SERIES
	RELEASE APPROV BAP		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 270 SERIES	DWG NO 0102-00-1041 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A-3294

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, RACK SLIDES	0102-00-1042	WVTK	0102-00-1042	1
NONE	EAR, RACK SLIDE	270-7073	WVTK	1400-00-7073	2
NONE	EAR, RACK SLIDE	270-7083	WVTK	1400-00-7083	2
NONE	SPACER, SLIDE	270-5503	WVTK	1400-01-5503	2
NONE	SLIDES REF: 2400-99-0002	110GD-20-1	NL	2400-07-0002	2
NONE	NUT, HEX, CAD I, 8-32	8-32 HEX NUT	CMRCL	2800-14-8100	8
NONE	SCREW, TRUSS HD, CROSS RECESS, 10-32X3/8	10-32 X 3/8	CMRCL	2800-20-0106	6
NONE	WASHER, FLAT, #8	#8 FW	CMRCL	2800-26-8000	8
NONE	SCREW, PAN, CAD I, CROSS RECESS, 8-32 X 3/8	8-32 X 3/8 PAN	CMRCL	2800-38-8106	8
NONE	LOCKWASHER, #8 SPLIT RING BIN 540	#8SRLW	CMRCL	2800-42-8000	8

WAVETEK PARTS LIST	TITLE: MODEL 270 SERIES RACK SLIDE KIT	ASSEMBLY NO. 1101-00-1042	REV A
		PAGE 1	

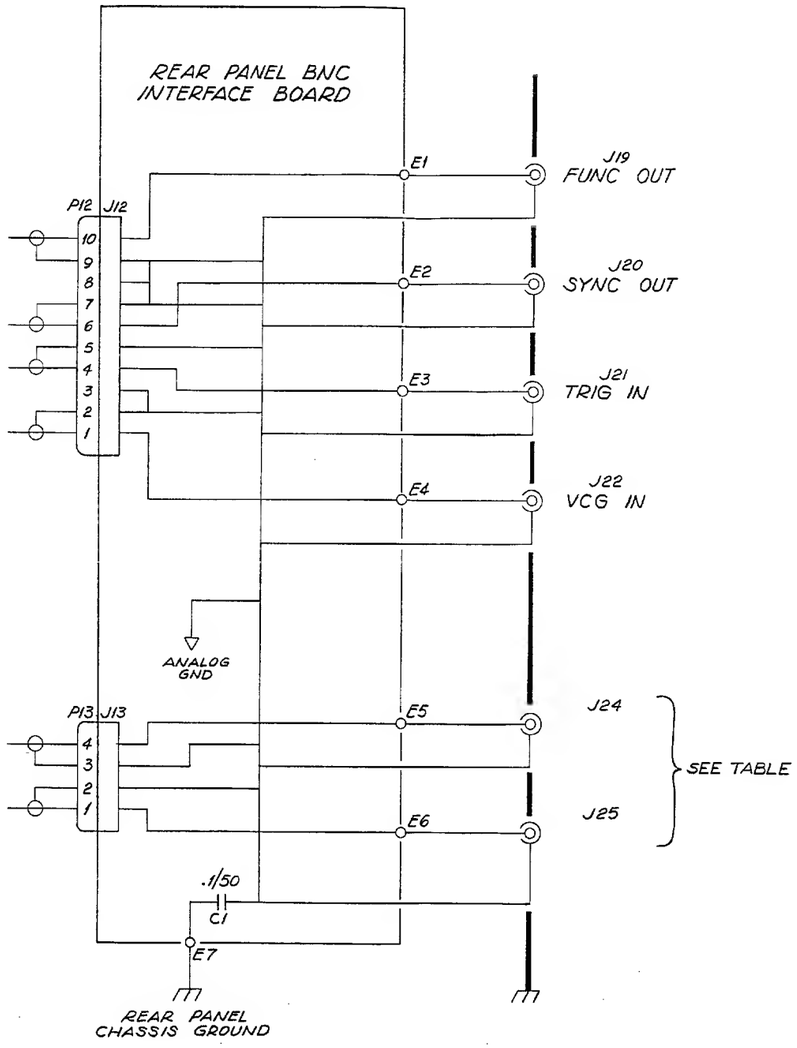


TYP BOTH SIDES

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 9-30-82	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RBL	9/15/83	TITLE: ASSEMBLY, RACK SLIDE
	RELEASE APPROV BD		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 0102-00-1042 REV
	SCALE	LOCI IDENT 23338	SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	# 3904	SC	8/8/83	



TABLE

MODEL	CONNECTOR	LABEL
270	J24	N/A
	J25	N/A
271	J24	N/A
	J25	N/A
273	J24	MARKER OUT
	J25	HORZ/GCV OUT
275	J24	ARB RTS/HOLD IN
	J25	ARB SYNC OUT
278	J24	REF IN
	J25	REF OUT

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, REAR PANEL BNC BOARD	0101-00-1010	WVTK	0101-00-1010	1
NONE	SCHEMATIC, REAR PANEL BNC BOARD	0103-00-1010	WVTK	0103-00-1010	1
NONE	ASSY, PC BD PREPPED 271-002-1010	271-002-2609	WVTK	1208-00-2609	1
C1	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	1
6	CONN, HEADER 10 PIN	102202-7	AMP	2100-02-0132	1
2	TERM, LOCK LUG	1414-8	SMITH	2100-04-0010	1

WAVETEK PARTS LIST | TITLE PCA, REAR PANEL BNC | ASSEMBLY NO. 1100-00-1010 | REV

PAGE 1

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN FN AQUINO 9/2/82	WAVETEK SAN DIEGO, CALIFORNIA	
MATERIAL	PROJ ENGR RBA 9/5/83	TITLE OPTION 002 REAR PANEL BNC'S	
FINISH WAVETEK PROCESS	RELEASE APPROV BHA	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030	
	DO NOT SCALE DWG	SCALE	MODEL NO 270 SERIES / DWG NO. 0103-00-1010 / REV A
		CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3814

APPENDIX A
AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE (ASCII)

b7 b6 b5 / BITS					0_0	MSG[1]	0_1	MSG	0_1	MSG	0_1	MSG	1_0	MSG	1_0	MSG	1_1	MSG	1_1	MSG
b4	b3	b2	b1	column / row	0		1		2		3		4		5		6		7	
0	0	0	0	0	NUL		DLE		SP	MLA ASSIGNED TO DEVICE	0	MLA ASSIGNED TO DEVICE	@	MTA ASSIGNED TO DEVICE	P	MTA ASSIGNED TO DEVICE	\	MEANING DEFINED BY PCG CODE	p	MEANING DEFINED BY PCG CODE
0	0	0	1	1	SOH	GTL	DC1	LLO	!		1		A		Q		a		q	
0	0	1	0	2	STX		DC2		"		2		B		R		b		r	
0	0	1	1	3	ETX		DC3		#		3		C		S		c		s	
0	1	0	0	4	EOT	SDC	DC4	DCL	$		4		D		T		d		t	
0	1	0	1	5	ENQ	PPC[3]	NAK	PPU	%		5		E		U		e		u	
0	1	1	0	6	ACK		SYN		&		6		F		V		f		v	
0	1	1	1	7	BEL		ETB		'		7		G		W		g		w	
1	0	0	0	8	BS	GET	CAN	SPE	(		8		H		X		h		x	
1	0	0	1	9	HT	TCT	EM	SPD	)		9		I		Y		i		y	
1	0	1	0	10	LF		SUB		*		:		J		Z		j		z	
1	0	1	1	11	VT		ESC		+		;		K		[		k		{	
1	1	0	0	12	FF		FS		,		<		L		\		l		|	
1	1	0	1	13	CR		GS		-		=		M		]		m		}	
1	1	1	0	14	SO		RS		.		>		N		^		n		~	
1	1	1	1	15	SI		US		/		?	UNL	O		_	UNT	o		DEL	

ADDRESSED COMMAND GROUP (ACG)

UNIVERSAL COMMAND GROUP (UCG)

[4] LISTEN ADDRESS GROUP (LAG)

TALK ADDRESS GROUP (TAG)

PRIMARY COMMAND GROUP (PCG)

SECONDARY COMMAND GROUP (SCG)

[1]MSG = INTERFACE MESSAGE
[2]b1 = DIO1 . . . b7 = DIO7
[3]REQUIRES SECONDARY COMMAND
[4]DENSE SUBSET (COLUMN 2 THROUGH 5)

DC4	=	DCL	Device clear	Universal Command Group
DC1	=	LLO	Local lockout	
NAK	=	PPU	Parallel poll unconfigure	
EM	=	SPD	Serial poll disable	
CAN	=	SPE	Serial poll enable	
SOH	=	GTL	Go to local	Addressed Command Group
EOT	=	SDC	Selected device clear	
ENQ	=	PPC	Parallel poll configure	
BS	=	GET	Group execute trigger	
HT	=	TCT	Take control	

APPENDIX B
PROGRAMMING COMMAND SUMMARY
(Excluding GPIB Command Groups Given in Appendix A).

Control and Data Names	Model 278 Key	ASCII Character (GPIB)
Change Sign	+/–	–
Decimal Point	•	•
0, 1, 2, . . . 9	0, 1, 2, . . . 9	0, 1, 2, . . . 9
Amplitude	AMPL	A
Mode	MODE	B
Function	FUNC	C
Offset	OFST	D
Exponent	EXP	E
Frequency	FREQ	F
External Trigger	EXT	G
Manual Trigger Released (Gate Off)	MAN (Released)	H
Execute	EXEC	I
Manual Trigger Pushed	MAN (Pressed)	J
Store Setting	STOR	M
Width	WID	N
Output On/Off	ON	P
Trigger Slope	SLP	Q
Burst	BRST	R
Period	PER	S
Trigger Rate	RATE	T
Upper Level	UPR	U
Lower Level	LWR	V
Recall Setting	RCL	Y
Reset	RST	Z
Percent Frequency	_____	XF
Get Mode	_____	XG
Trigger Level	LVL	XL
SRQ Mode	_____	XQ
Talk Mode	_____	XT
Recall Next Lesser Numbered Program	_____	XU
Terminator	_____	XV
Recall Next Greater Number Program	_____	XW
Cursor	↑, ↓, ←, →	_____
Clear Entry	CLR	_____
Beep On/Off	♪	_____
Display Test	DISP TEST	_____
Status Display	STAT	_____
Service Request	SRQ	_____
GPIB Address	ADRS	_____
Command Recall	CMD RCL	_____
Return to Local	LCL	_____

APPENDIX B (Cont)

Function (C) Code

0 Sine
1 Triangle
2 Square
3 Square Complement
4 DC
5 External Width
6 Pulse
7 Pulse Complement

Main Generator Mode (B) Code

0 Continuous
1 Triggered
2 Gated
3 Burst
4 Synthesized
5 TTL Reference
6 Zero Reference
7 TTL Lock
8 Zero Lock

Output On/Off (P) Code

0 Output Off
1 Output On
2 Output Off, LO Z

Trigger Slope (Q) Code

0 Positive Edge
1 Negative Edge

Trigger Source (G) Code

0 External Triggering
1 Internal Triggering

GET Mode (XG) Codes

NOTE: This parameter selects which kind of action the 278 will take when it receives a GET command.

0 Execute and Trigger Upon Receipt of GET Command (No Error Checking).
1 Fetch Next Stored Setting, Execute and Trigger Upon Receipt of GET Command (No Error Checking).
−1 Fetch Previous Stored Setting, Execute and Trigger Upon Receipt of GET Command (No Error Checking).

SRQ (XQ) Code

NOTE: This parameter selects the conditions under which the SRQ line is asserted. Value can be 0 through 255. The equivalent binary value selects the response conditions as shown in table B-1 example. Binary 1 = Selected, Binary 0 = Not Selected.
XQ1 *is the SRQ power-up mode. (The rsv bit is always asserted selected or not.)*

Talk Message (XT) Code

NOTE: This parameter selects the kind of message the 278 will send when it is addressed as a talker on the GPIB.

0 Programming Error list (only errors from GPIB input). 0 is the power-up talk mode. A typical error string is E 1F 2AD 3Y. Some error string characterics are:

a. All error strings begin with E.
b. Most recent error is at the end of string.
c. Errors are separated by blanks.
d. Class 1 Errors: A 1 followed by programming character that caused the error.
e. Class 2 Error: A 2 followed by the two conflicting program characters.
f. Class 3 Error: A 3 followed by M (Store) or Y (Recall).
g. Error strings can be up to 80 characters including E and blanks.
h. After transfer, the instrument clears the error string.

1 Poll Byte Response: The byte sent if a serial poll was performed. The controller, upon reading this byte, clears the poll byte and resets the SRQ line if asserted.

2 The most recently selected parameter and its value. Example: FREQ 1E3. If no parameter is selected; e.g., power-on state or reset, then returns: NO PARAMETER SELECTED.

APPENDIX B (Cont)

3 The entire instrument setup after last execute. Example: F1E3A5D0B0C0R2S1E-3N45E-9U2.5V-2.5G0T200P0Q0XL1.5 (This string is returned in the reset condition.)

4 The instrument setup when executed is received; same format as XT3.

5 Instrument Identification: WAVETEK MODEL 278 V(x.x). x.x identifies the software version number.

6 The time since the instrument was powered on. Example Time: 1.3. Unit of measure is hours with 0.1 hour resolution (6 minutes).

7 The accumulated operating time. Example: TOTAL TIME: 306.2.

NOTE:

Toggling switch 7 (figure 2-2) clears the instrument-operating-time clock. With SW7 on, the clock runs during power on. With SW7 off, the clock clears to zero.

8 The number of stored settings installed. For the 278: STORED SETTINGS 100.

Table B-1
Serial Poll Response Byte

Bit Weight	**128 (MSB)**	**64**	**32**	**16**	**8**	**4**	**2**	**1 (LSB)**
Bit Meaning	SRQ Key (Front Panel)	rsv	Reference Not Locked	Undefined	Low Battery	Fuse Blown	Output Protection	Program Error
Example*	1	0	0	0	0	0	0	1

Select Program Error and SRQ key (XQ129**)*

APPENDIX C
DISPLAYS

Under remote operation, certain characters may appear in the extreme right side of the display. Those characters are:

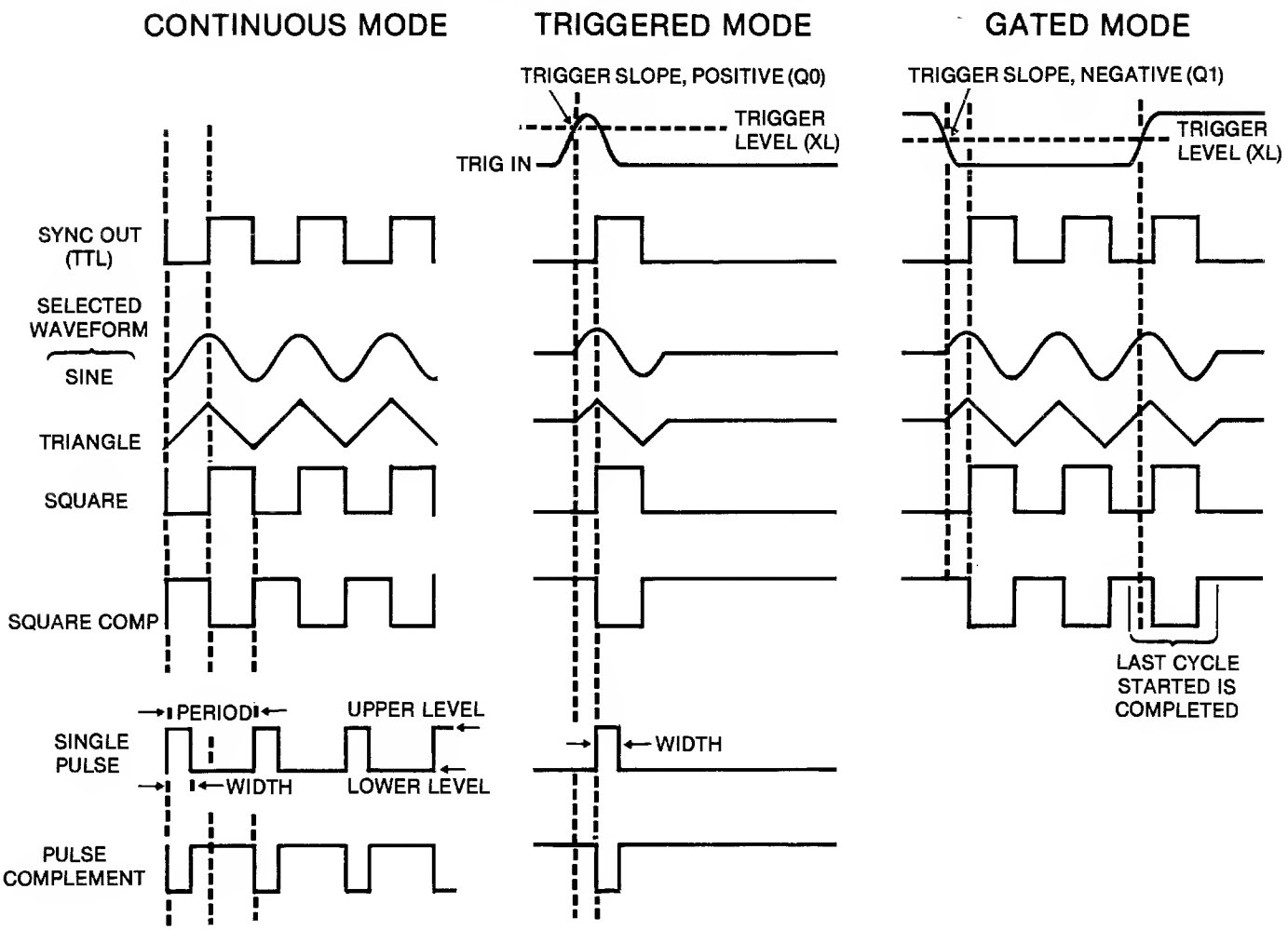
R — Remote
L — Addressed to Listen
T — Addressed to Talk
Q — Request for service because of selected SRQ code.

Key Pressed	Display - ACTUAL (Explanation)
ADRS	GPIB ADRS (Decimal address)
AMPL	AMPLITUDE (Value) (mV or V)
(beep)	(Audible beep)
BRST	BURST COUNT (Value)
CLR	(Clears any unexecuted numerical entry of the last parameter entered)
CMD RCL	(A string of letters and numbers up to 40 characters long displayed 20 characters at a time and shifted by the cursor ←, →)
CURSOR ←, →	(If a value is being displayed, the selected digit blinks. If there is no value being displayed, there is no effect. If it was a command recall, ← shifts the display four characters to the left. If it was a command recall, → shifts the display four characters to the right.
CURSOR ↑	(If the display is a value, code or storage location number, it increments.)
CURSOR ↓	(If the display is a value, code or a storage location number, it decrements.)
DISP TEST	(All display segments are lit.)
EXEC	EXECUTE (If no class 1 errors)
EXP	(If previous display was a value or a code, it is suffixed with an E.)
EXT	EXTERNAL TRIGGER (0) or INTERNAL TRIGGER (1)
FREQ	FREQ (Value) (mHz, Hz, kHz or MHz)
FUNC	FUNC (Function) (Code)
LVL	TRIG LEVEL (Value) (mV or V)
LCL	LOCAL or LOCAL LOCKOUT ON (on remote)
LWR	LOWER LEVEL (+ or −) (Value) (mV or V)
MAN TRIG	(When pressed: No display if in continous mode, TRIGGER if in any triggered or burst mode, GATE if in gated mode.

APPENDIX C (Cont)

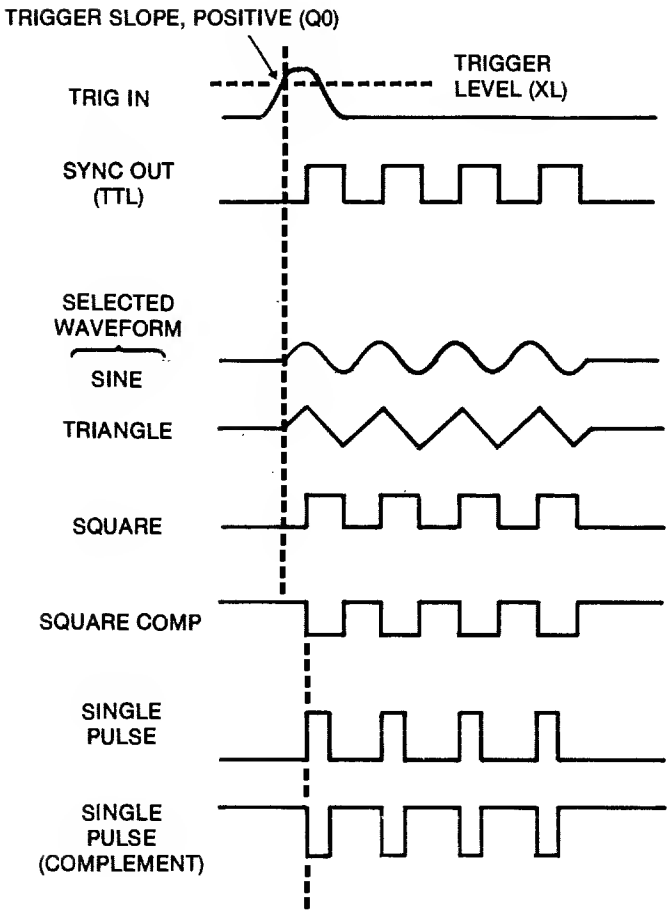
Key Pressed	Display - ACTUAL (Explanation)
MODE	MODE (CONTINUOUS (0), TRIGGERED (1) or GATED (2), BURST (3), SYNTHESIZED (4), TTL REF (5), ZERO REF (6), TTL LOCK (7), ZERO LOCK (8))
ON	OUTPUT (OFF (0); ON (1); or OFF, LO Z(2))
OFST	OFFSET (+ or −) (Value) (mV, V)
PER	PERIOD (Value) (ns, μs, ms, or s)
RATE	TRIG RATE (Value) (Hz, kHz, or MHz)
RCL	No. (Value) LAST RECALLED
RST	RESET or UNIT REMOTE (if in remote)
SLP	TRIG SLOPE (POS (0) or NEG (1))
SRQ	SRQ NOT ENABLED or SRQ ASSERTED (Proper SRQ selected)
STOR	No. (Value) LAST STORED
STAT	(Display changes automatically) FREQ (Value) (mHz, Hz, kHz or MHz) AMPLITUDE (Value) (mV or V) OFFSET (Value) (mV or V) MODE (Mode) (Code) FUNC (Function) (Code) BURST COUNT (Value) PERIOD (Value) (ns, μs, ms, or s) WIDTH (Value) (ns, μs, or ms) UPPER LEVEL (+ or −) (Value) (mV or V) LOWER LEVEL (+ or −) (Value) (mV or V) OUTPUT (OFF (0); ON (1); or OFF, LO Z(2)) EXTERNAL TRIGGER (0) or INTERNAL TRIGGER (1) TRIG RATE (Value) (Hz, kHz, or MHz) TRIG SLOPE (POS or NEG) (Code) TRIG LEVEL (+ or −) (Value) (mV or V)
UPR (Number key)	UPPER LEVEL (+ or −) (Value) (mV or V) (Number corresponding to the selected key.)
WID	WIDTH (Value) (ns, μs, or ms)

APPENDIX D
OUTPUT AND TIMING FOR MODES AND FUNCTIONS



APPENDIX D (Cont)

BURST MODE



NOTE: NUMBER OF CYCLES IS PROGRAMMED (1 THROUGH 1,048,200)

APPENDIX E
Glossary of Mnemonics

Microprocessor/Power Supply Board

AD0 to AD7	Bidirectional, multiplexed, 8 bit address/data bus from/to microprocessor
ADR0 to ADR15	16 bit address bus from microprocessor-lower 8 bits are latched from AD0 to AD7
$\overline{\text{ANA0}}$ to $\overline{\text{ANA3}}$	4 line address decoding for analog control lines to function generator and synthesizer board
$\overline{\text{ANALOG}}$	Decode line for analog section of memory
ANL0 to ANL27	28 analog logic signals to function generator board
$\overline{\text{AR0}}$ to $\overline{\text{AR3}}$	4 line address decoding to analog registers for function generator board control lines
AS	Address strobe from microprocessor
ATN	IEEE-488 "attention"
BADR0 to BADR2	3 buffered address lines to synthesizer board
BATV	Battery voltage
BDATA0 to BDATA7	8 bit, buffered, latched data bus to synthesizer board
D101 to D108	8 bit, IEEE-488 data bus
DAC	IEEE-488 "data accepted"
DATA0 to DATA7	8 bit, latched data bus for control lines to the display, sample and hold, and analog interface
DAV	IEEE-488 "data valid"
$\overline{\text{DISP}}$	Decode line for display section of memory
E	Enable line from microprocessor
EOI	IEEE-488 "end or identify"
FPADEN	Front panel GPIB address entry switch
GA0 to GA4	GPIB address switches corresponding to 2^0 through 2^4 respectively. (1 through 16) adding to 31 maximum
$\overline{\text{GPIB}}$	Decode line to select the IEEE-488 interface (general purpose interface bus)
IFC	IEEE-488 "interface clear"
$\overline{\text{KYBD}}$	Decode line to select keyboard
$\overline{\text{MR}}$	Master reset to initialize microprocessor
$\overline{\text{NMI}}$	Non-maskable interrupt line to microprocessor
PORT 10 to PORT 17	8 line I/O port 1 to/from microprocessor
PORT 20 to PORT 24	5 line I/O port 2 to/from microprocessor
$\overline{\text{RAM1}}$ & $\overline{\text{RAM2}}$	Address decode lines for random access memory IC's 1 and 2
REN	IEEE-488 "remote enable"
RFD	IEEE-488 "ready for data"
$\overline{\text{ROM1}}$ to $\overline{\text{ROM2}}$	Address decode lines for read-only memory IC's 1 and 2
R/$\overline{\text{W}}$	Read/write line from microprocessor
SH0 to SH3	4 sample-and-hold analog signals to function generator board

APPENDIX E (Cont)

SRQ	IEEE-488 "service request"
TEST	Control line to allow operation with external test program—not normally used
$\overline{\text{WRP}}$	Write pulse to RAM

Display Board (Excluding Mnemonics Common to Microprocessor/Power Supply Board)

ANOA to ANOO & ANODP	Vacuum florescent display anodes corresponding to 14 segments, comma, and and decimal point, respectively
$\overline{\text{BLANK}}$	Blanking control for display and scan clock
DSP	Display synchronizing pulse for shift register scan
GRID 1 to GRID 20	Display grids controlling each digit

Function Generator Board

AMP	Analog control voltage for amplitude (SH1)
AMPLDC	XY multiplier feedback of amplitude control dc test line
$\overline{\text{CPM}}$	Capacitance multiplier select line (ANL15)
$\overline{\text{DCA}}$	DC amplifier select line (ANL13)
DCCOMP	DC compensation and low frequency linearity correction for triangle buffer test line
EXW	External width select line (ANL18)
$\overline{\text{FR0}}$ to $\overline{\text{FR7}}$	Frequency range select lines to range capacitors, capacitance multiplier, and frequency compensation (ANL0 to ANL7)
FRQ	Analog control voltage for frequency (SH0)
FUB	Signal to microprocessor that output fuse is blown (PORT11)
MC0 & MC1	2 mode control lines (ANL11 and ANL12)
OA0 & OA2	2 output attenuator control lines (ANL8 and ANL10)
OAP	signal to microprocessor that the output amplifier protection circuit is operating (PORT 10)
OST	Analog control voltage for offset (SH2)
$\overline{\text{OVR}}$	Frequency overrange select line (ANL14)
PATEST	Preamplifier output test line
PLS	Pulse input select line (ANL25)
$\overline{\text{PLS}}$	Pulse complement select line (ANL24)
PLSI	Pulse input from auxiliary board
$\overline{\text{RCT}}$	Rectangular waveform select line—square or pulse (ANL23)
$\overline{\text{SIN}}$	Sine wave select line (ANL21)
SQB	Output from square buffer
SQR	Square wave select line (ANL20)
$\overline{\text{SQR}}$	Square complement select line (ANL19)
SQS	Square buffer to square logic signal
THC	Trigger holding current
TRB	Triangle buffer output
TRGI	Trigger input from synthesizer board
TRGO	Trigger output to synthesizer board
$\overline{\text{TRI}}$	Triangle wave select line (ANL22)
TRITST	Triangle buffer output test line

APPENDIX E (Cont)

TRL — Analog control voltage for trigger level (SH3)

TRN — Triangle generation current node

VCGI — Voltage control generation circuit input from synthesizer board

VCGO — Voltage control generation circuit output to synthesizer board

VCGTST — Voltage control generation circuit test line

VCV — Voltage control generation circuit voltage ouput

XYI — X-Y multiplier input

+I — Tracking current (I) source from VCG

−I — Tracking current (I) sink to VCG

+TR — Rising edge trigger select line (ANL 17)

−TR — Falling edge trigger select line (ANL 16)

Synthesizer Board

ANALOG INTERFACE (J15) — A connector which allows exchange of analog information between the synthesizer and function generator boards.

- J15-2 VCG summing node (see VCGI)
- J15-4 VCG output (see VCGO)
- J15-7 Count enable line from the Burst Counter to control the analog waveform in burst (see TRGI).
- J15-9 External trigger (see TRGO).
- J15-13 Square wave input to the synthesizer board (see SQS).

AUX POWER (J17) — The dc power input the synthesizer board.

BINARY A, BINARY B — Control lines that select the binary divider output (U32).

B0-B19 — Data lines that load the burst counters U9-U13.

BURST — The burst counter control line. A low disables the counter, while a high enables it.

$\overline{\text{BURST}}$ — Complementary burst counter control line.

CLOCK — A control line that sequences data into the PLL chip U21.

DATA — A dynamic control line which sets data into the PLL 16 bit serial shift register (U21). The data is the value of the PLLs internal divide-by N counter.

DECADE A, B, and C — Static control lines that selects the decade range from the Synthesizer Frequency Dividers. See below:

Decade C	Decade B	Decade A	Synthesized Output Frequency
0	0	0	10-24 MHz
0	0	1	1-10 MHz
0	1	0	100k-1 MHz
0	1	1	10k-100 kHz
1	0	0	1k-10 kHz
1	0	1	100 Hz-1 kHz
1	1	0	10 Hz-100 Hz
1	1	1	1 Hz-10 Hz

DIGITAL INTERFACE — The data interface between the microprocessor and synthesizer boards.

- J16-1 to J16-8 Tristate data lines that supply data for the control logic registers (U2-U7)
- J16-9 to J16-11 Address lines from the microprocessor to the control logic address decoder (U1), which sequences the address strobe from J16-12 to select control registers U2 through U7.
- J16-12 $\overline{\text{ANA2}}$ strobes the address into the address decoder (U1).
- J16-20 Lock detect (see LOCK DETECT).

ENABLE — A dynamic control line that transfers data from PLL's shift register (U21) to its divide-by-N counter.

APPENDIX E (Cont)

F_O — A signal line from the VMP circuit (U28-15) to the phase lock input (U21-9). Frequency can vary from 1 to 2.4 MHz.

$\overline{\text{INTER-}}$ NAL REF — A static control line that selects either the internal or external reference source. A low selects the internal reference, while a high selects the external reference.

INT/$\overline{\text{EXT}}$ TRIG — A control line that selects either the internal or external trigger source. A low selects external trigger (TRGO). A high selects the internal synthesizer as the trigger source.

LOCK DET — A static line that indicates status of the main synthesizer loop. A high indicates the main loop is locked, while a low indicates loop not locked.

ϕ LOCK IN — A signal line from the reference input comparator (U16-4) to the main loop selector switch (U37-13). It is enabled when SYNTH/$\overline{\phi}$ SELECT goes low.

REF INPUT (A front panel BNC) — The external input for external reference or phase lock applications.

REF LEVEL SELECT — A static control line that selects the trigger level of the reference input comparator (U16). A low allows the comparator to trigger with a 700 mVp-p signal, while a high allows triggering at approximately +1.6V.

REF OUT (A front panel BNC) — An output from the synthesizer board to the front panel. Output signal depends upon the mode:
Synthesized — 10 MHz
Internal Trigger — Programmed trigger rate.

SQS — The square wave output from the function generator board. It clocks the burst counter and provides the phase lock signal to the main loop.

SYNTH/$\overline{\phi}$ SELECT — A static control line that selects the reference input to the main loop. A low selects Phase LOCK IN and disables the divide-by-N counter (U26). A high selects the output from the decade divider (U36).

SYN/$\overline{\text{REF}}$ — A static control line that selects the reference source for the Reference Output circuit.

TRGO — The buffered external trigger input from the function generator board.

TRGOB — A trigger line to the burst counter that is controlled by the INT/$\overline{\text{EXT}}$ TRIG line.

VCO — The 10 MHz to 24 MHz output from the VCO circuit.

VCGI — The VCG control voltage output from the main loop.

VCGO — An analog level that is summed at the main loop output.

$\overline{\text{VCG}}$ — A static control line which connects or disconnects the main loop output from the VCG summing node. A low enables U47A and U47D, and disables U47C, while a high disables U47A and U47D, and enables U47C.

VMP SET — A pulse that clears the VMP circuit for a new VMP cycle at the beginning of a lock cycle.

VMP0-VMP3 — Static control lines which preloads the VMP counter U29. See the following table.

PROGRAMMED 5TH DIGIT	VMP3	VMP2	VMP1	VMP0
0	0	1	1	0
1	0	1	0	1
2	1	1	1	0
3	1	1	0	1
4	1	1	0	0
5	1	0	1	1
6	1	0	1	0
7	1	0	0	1
8	1	0	0	0
9	0	1	1	1

APPENDIX E (Cont)

10 Hz-99.9 Hz	A static control line that causes a decrease in curent to the main loop charge pump on the 10 to 99.9 Hz range.
$\overline{\text{10 Hz-999 Hz}}$	A static control line that selects the 10 to 999 Hz main loop filter range capacitor. A low enables U45B.
$\overline{\text{1k-9.99k}}$	A static control line that selects the 1k to 9.99 kHz main loop range capacitor. A low enables U45C.
$\overline{\text{10k-99.9k}}$	A static control line that selects the 10k to 99.9 kHz main loop filter range capacitor. A low enables U45D.
$\overline{\text{100k-12 MHz}}$	A static control line that selects the 100k to 12 MHz main loop filter range capacitor. A low enables U45A.

APPENDIX F
WAVEFORM MEASUREMENTS

Frequency Jitter Measurement

Frequency jitter is defined as the cycle to cycle variation in period. Using a scope (with time base multiplier) display a square wave such that one cycle covers more than half the display (see figure F-1). Trigger the scope internally on the leading edge of signal. Using the time base multiplier expand the leading edge of the cycle after trigger by a factor of 100. Jitter is the peak to peak horizontal excursion of the displayed edge (see figure F-2). % jitter is given by:

$$\% \text{ Jitter} = (\text{Jitter/Period}) \times 100$$

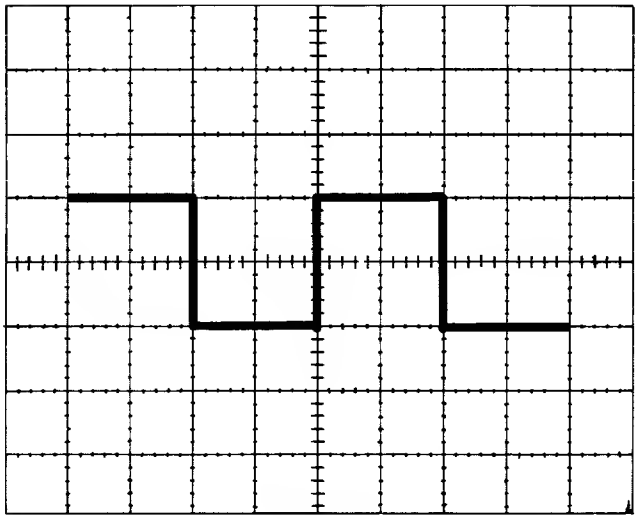


Figure F-1.

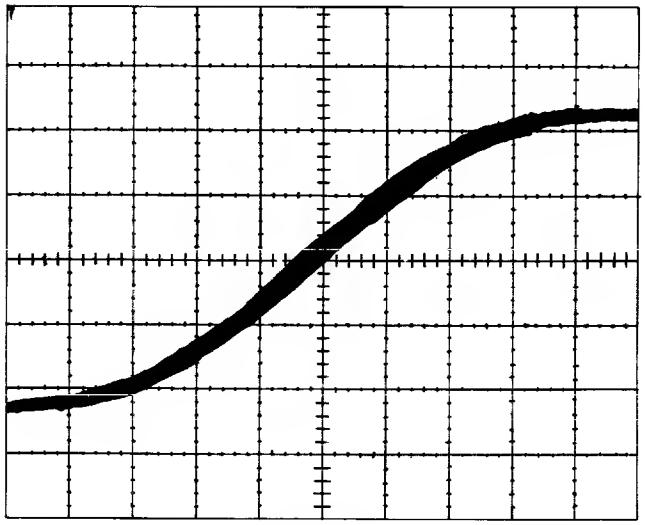


Figure F-2.

This test method is accurate for jitter caused by random or non-coherent noise sources. Coherent (harmonically related) cycle-to-cycle jitter requires unique verification.

Amplitude Measurements

There are several factors to be considered when making amplitude measurements. The type of DVM, the frequency range over which the meter is accurate, and the accuracy of the 50Ω load used for termination are the most important.

1. There are three basic types of DVM's: Averaging, true rms, and averaging scaled. The readings obtained can vary by more than 10% depending on DVM type and the waveform. The correct readings (related to volts peak to peak) are given below for each type of meter and each waveform.

   Average Reading:

Function	Reading
Sine	Vp-p/π
Triangle	Vp-p/4
Square	Vp-p/2

   True RMS:

Function	Reading
Sine	Vp-p/2$\sqrt{2}$
Triangle	Vp-p/2$\sqrt{3}$
Square	Vp-p/2

   Averaging Scaled: This type of meter measures internally like an average reading meter, but the displayed reading is scaled (multiplied by a constant) to read like a true rms meter. This scaling technique only works on sine waveforms; however, it gives less obvious results for other waveforms. The correct readings are given below:

Function	Reading
Sine	Vp-p/2$\sqrt{2}$
Triangle	(Vp-p × 1.1107)/4
Square	(Vp-p × 1.1107)/2
	or
Triangle	(Vp-p/4) × 1.1107
Square	(Vp-p/2) × 1.1107

2. Most ac volt meters have a relatively limited range of frequencies over which the meter is most accurate. For most meters this range is

about 500 Hz-5 kHz. In order to make accurate measurements the basic accuracy of the meter in its specified frequency operating range should be less than 0.2%.

3. The 50Ω load used to terminate the signal being measured can also introduce significant errors into the amplitude accuracy measurement. In general the measurement will be in error by 1/2% for every 1% error in the load. Standard loads available from Tektronix are ±2% accuracy. Therefore up to 1% error in amplitude measurement can result when using these loads. It is recommended to use a 0.1% accurate termination or to compensate the readings obtained based on the actual load value. The method for doing this is given below.
   a. Let R be the value of the termination.
   b. Let K be the correction factor applied to the DVM reading:

      Then: (correct reading) = (DVM reading) × K

      where $K = \frac{R+50}{2R}$

   Using this method the load tolerance can be ±5%.

Symmetry Measurements

1. Symmetry defined as a percentage is the ratio of positive half cycle time to the period (see figure F-3):

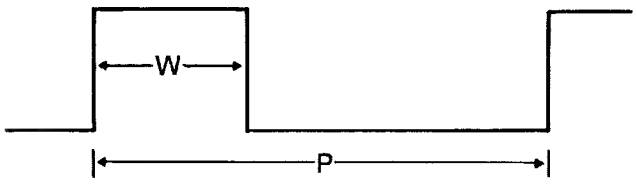


Figure F-3.

Where: % symmetry = (W/P) × 100

2. Symmetry error is, therefore, the difference from 50% symmetry:

   % Symmetry Error = [(½P—W)/P] × 100

3. When using a scope and alternately triggering on + and − slope of signal the symmetry error measured is twice the actual error. Therefore, when using this method the measured error must be divided by 2. Also, this method is only accurate at frequencies where the rise and fall time is not a significant part of the period. The period should be about 1000 times greater than the rise/fall time. This is about 10 μs or 100 kHz.
4. To measure symmetry at 12 MHz a different technique must be used. Connect signal (terminated into 50Ω) to a sampler set at 10 ns/div. Upper and lower levels should be exactly centered about horizontal centerline on scope display (see figure F-4). Rising edges of first and second cycle should be exactly equidistant from vertical center line. The distance of the falling edge from the vertical center line at the point falling edge crosses horizontal center line is the symmetry error.

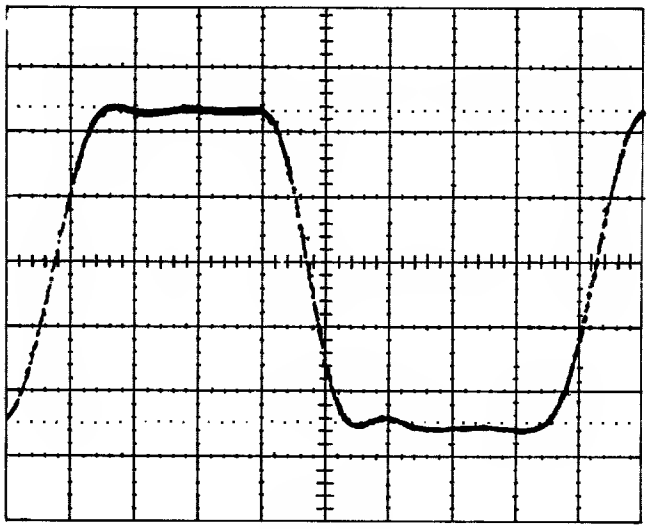


Figure F-4.

Waveform Quality Measurement

Waveform quality measurements should always be made using a sampling oscilloscope with precision 50Ω termination and cabling. Standard RG58 coax cable is not good enough for waveform quality measurements. Percent aberration is the ratio of absolute peak-to-peak variation from the 0% (negative level) or 100% (positive level) point on the square waveform to the absolute peak-to-peak amplitude of the square wave. See figures F-5, F-6 and formula shown below. In order to get an accurate display the top (or bottom) of the waveform should be expanded both vertically and horizontally to fill the scope display. The pictures below were made on a 5 Vp-p square waveform at 3 MHz and the scope horizontal and vertical were set to 20 ns/div and 100 mV/div respectively. Also, best

results are obtained when using the low noise (averaging) setting on the sampling scope.

$$\% \text{ ABERRATION} = \frac{|\text{PK} - \text{PK VAR}|}{|\text{PK} - \text{PK SQWA}|} \times 100$$

SQWA = SQUARE WAVE AMPLITUDE

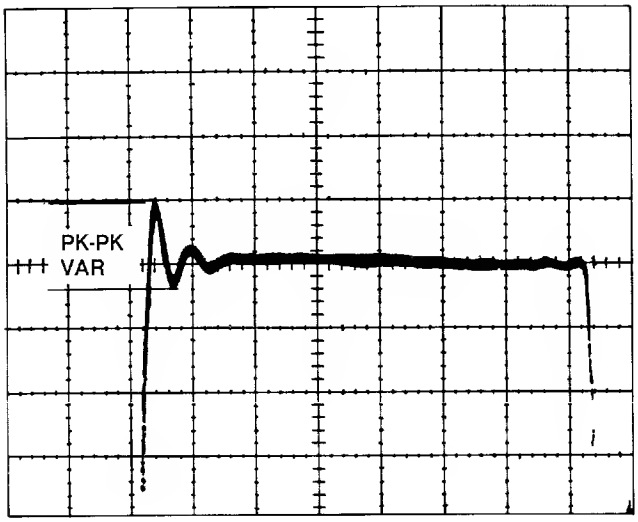


Figure F-5.

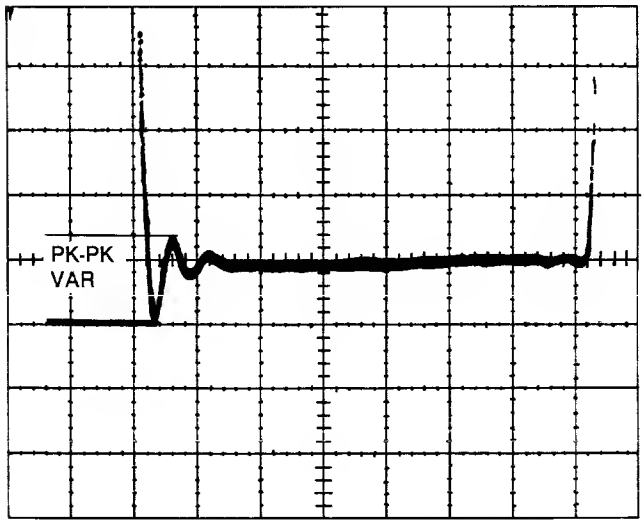


Figure F-6.

Width Measurement

Width is measured from the 50% point of the leading edge of the pulse to the 50% point of the trailing edge (see figure F-7). The pulse at the function out must be loaded into 50Ω.

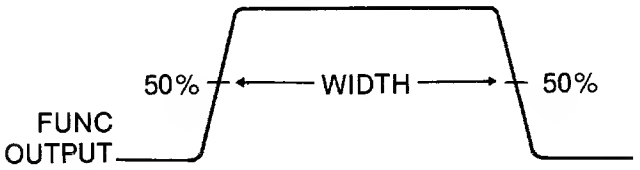


Figure F-7.

Width Duty Cycle Definition

Defined as a percentage, width duty cycle is the ratio of width to the minimum period that does not cause pulse dropout:

$$\% \text{ DUTY CYCLE} = (\text{WIDTH/MIN PERIOD}) \times 100$$

For example, if width were set to 100 ns and the minimum period that could be programmed before pulse dropout occurred was 163 ns then the duty cycle would be:

$$\% \text{ DUTY CYCLE} = (100\text{E-}9/163\text{E-}9) \times 100$$
$$\% \text{ DUTY CYCLE} = 61.3\%$$

Width Jitter Measurement

Width jitter is defined as the pulse to pulse variation in pulse width. Using a scope (with time base multiplier) display one pulse on scope display so the pulse covers at least half of display (see figure F-8). Scope must be triggered internally on leading edge of pulse (not sync out). Using the time base multiplier expand the trailing edge of pulse by a factor of 100. Jitter is measured as the peak to peak horizontal excursion of the trailing edge (see figure F-9). % Jitter is:

$$\% \text{ Jitter} = (\text{Jitter/Width}) \times 100$$

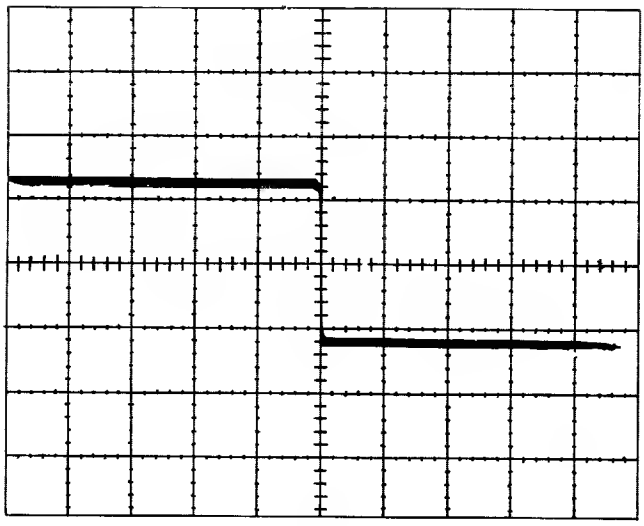


Figure F-8.

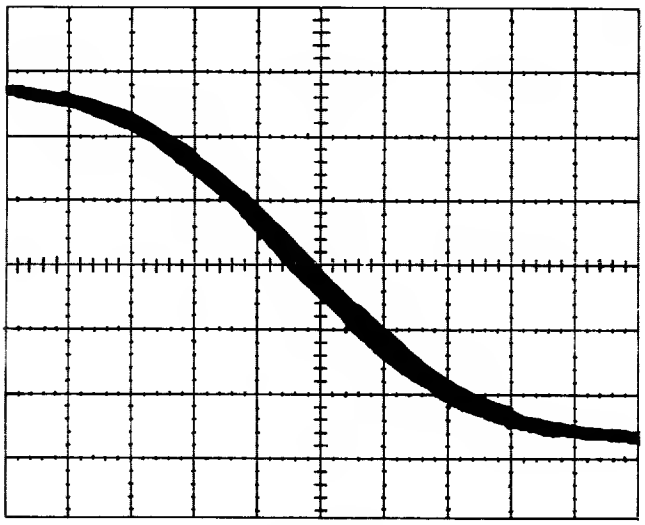


Figure F-9.